# Colour Television
# Chassis GR2.1

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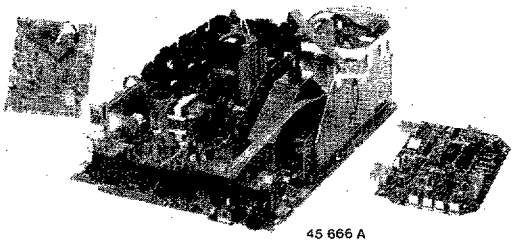

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# Circuit Description

## Contents



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Contents:



# 1. Introduction

The GR2.1 is a chassis for large-screen 21", 25" and 28" colour televisions. The GR2.1 will succeed the 21" stereo G90B, CP110 and G110.
Depending on the version of the television set, the chassis can process the systems PAL BG, PAL I, SECAM BG, SECAM LL' and SECAM DK. Depending on the version, the set may be equipped with 2 euroconnectors, a Y/C and an audio out connector. Teletext (TOP and/or FLOF) and Picture in Picture (PIP) are included in the possibilities.
The sub-functions: channel selector, videoprocessing, video check, audio output amplifiers, sync processing, frame and line circuits, operation and power supply are located on the carrier panel. The following functions are situated on separate modules:
- teletext;
- video and audio IF and audio processing;
- PIP;
- second euroconnector and PIP interfacing.

The chassis is operated by means of a menu-controlled operating system.

## 1.1 Service Facilities

### Test points

The GR2.1 chassis is fitted with test points (TP1, TP2, etc.) in the service printing on the component side of the carrier panel. These test points, which have also been included in the Service Manual, enable quick diagnosing.

### Service Default Mode

The software of the GR2.1 is equipped with the Service Default Mode. To activate this mode, the service pins on the carrier panel should be shorted when the set is switched on with the mains switch. An "S" will appear on the screen to indicate that the set is in the Service Default Mode. The set is now in a defined state.

### Error messages

The microcomputer contains an error detection system which, via OSD, sends error messages about defective circuits connected to the $I^2C$ bus.

## 1.2 Block Diagram

### Video input signals

The video signals can be presented in several ways (see Fig. 2.1). A high-frequency signal is supplied via the tuner, CVBS signals are presented via the two euroconnectors (EXT1 and EXT3), separated chrominance and luminance via the Y/C input (EXT2), and RGB via euroconnector EXT1.
The HF signal is demodulated into CVBS via the tuner and the video IF, which is located on the IF/audio panel. This CVBS signal is also presented to EXT1 and EXT3.

### Video source selection

The choice between CVBS from EXT1 and CVBS from EXT3 is made via switch 7802-2A. Switch 7000-2B chooses between CVBS from EXT1/3 and CVBS from the IF. Finally, switches 7312 make a choice between the CVBS signals selected and the chrominance (C) and luminance (Y) signals from EXT2. The luminance and chrominance paths begin at

# 2. The operating system

## Introduction

The GR2.1 chassis is operated by means of a single-chip microcomputer of type TMP47C1637 for stereo sets, and type TMP47IC1237 for mono sets. The diagram is shown in Fig. 2.1.

## Control keys

On the local keyboard are 5 keys which pass on a particular part of the +5 supply voltage, depending on which key has been pressed, to pin 14 of the microcomputer. This information is processed in the microcomputer via an analogue-to-digital converter. The various voltages are shown in table 2.1.

| P- | P+ | ◿ - | ◿ + | Install | (◿ -) + (P+) |
|---|---|---|---|---|---|
| 2V3 | 0V6 | 1V2 | 3V0 | 4V6 | 1V6 |

Table 2.1

The RC5 (enlarged) commands, originating from the remote control, are fed to pin 35 via infrared receiver 1003.
The basic functions, including several menus, can be operated via the local keyboard.

## Menu operation

A few non-basic functions are operated via a menu structure. This menu structure can be divided into three groups: the main menu, the installation menu and the service menu (see Service Manual).
The main menu is displayed with the menu on/off command on the remote control. The installation menu is displayed with the install command on the local keyboard, and the service menu by simultaneously pressing the ◿ - and P+ keys on the local keyboard after switching the set into the service default mode.

## $I^2C$ bus and error messages

The microcomputer communicates via the $I^2C$ bus with the PLL tuner, video control TDA4680, stereo decoder TDA8415/TDA8417, sound control TDA8425, the I/O expander on NICAM decoder PCF8574, the teletext decoder, the PIP module and the EEPROM, ST24CO2CP.
The following data is exchanged with the various devices:
- tuning data is sent to the tuner;
- data on contrast, brightness, colour saturation, white balance, peak-white limitation and cut-off point adjustment is sent to the video control;
- the stereo decoder receives switching data and transmits data on the sound mode (mono/stereo/dual);
- volume, treble and bass, and source selection data is sent to the sound control;
- the microcomputer receives data, via the I/O expander, on the NICAM sound mode;
- the teletext decoder receives and interprets all RC5 operating commands;
- all commands affecting the PIP picture are sent to the PIP module (no source selection commands);
- the data on personal preference (PP), tuning frequencies/system selection, options and picture tube settings are stored in the EEPROM.

In case of a communication error between the various circuits and the microcomputer, the microcomputer will generate an error message on the screen.

## System selection

The system switching voltages, which are present on pins 6, 7 and 8, activate the different sub-circuits which are needed with the various systems. Table 2.2 shows the various levels on the pins in combination with the various systems.

| SYSTEM | PIN MICROCOMPUTER | | |
|---|---|---|---|
| | 6<br>pos/neg | 7<br>L' | 8<br>I/BG |
| BG | 0V | 3V | 3V |
| PAL I | 0V | 3V | 0V |
| L | 3V | 3V | 0V |
| L' | 3V | 0V | 0V |

Tabel 2.2

## PIP source selection

PIP source selection takes place with the switching voltages on pins 12 and 19. The following signal sources may be selected: tuner, CVBS from EXT1 (euroconnector 1), CVBS from EXT2 (Y/C connector) and CVBS from EXT3 (euroconnector 2). Table 2.3 shows the various levels on the pins in combination with the various PIP sources.

| PIP SOURCE | PIN MICROCOMPUTER | |
|---|---|---|
| | 19<br>PIP 1 | 12<br>PIP 2 |
| TUNER | 0V | 0V |
| EXT1 | 0V | 0V6 |
| EXT2 | 8V5 | 0V |
| EXT3 | 8V5 | 0V6 |

Table 2.3

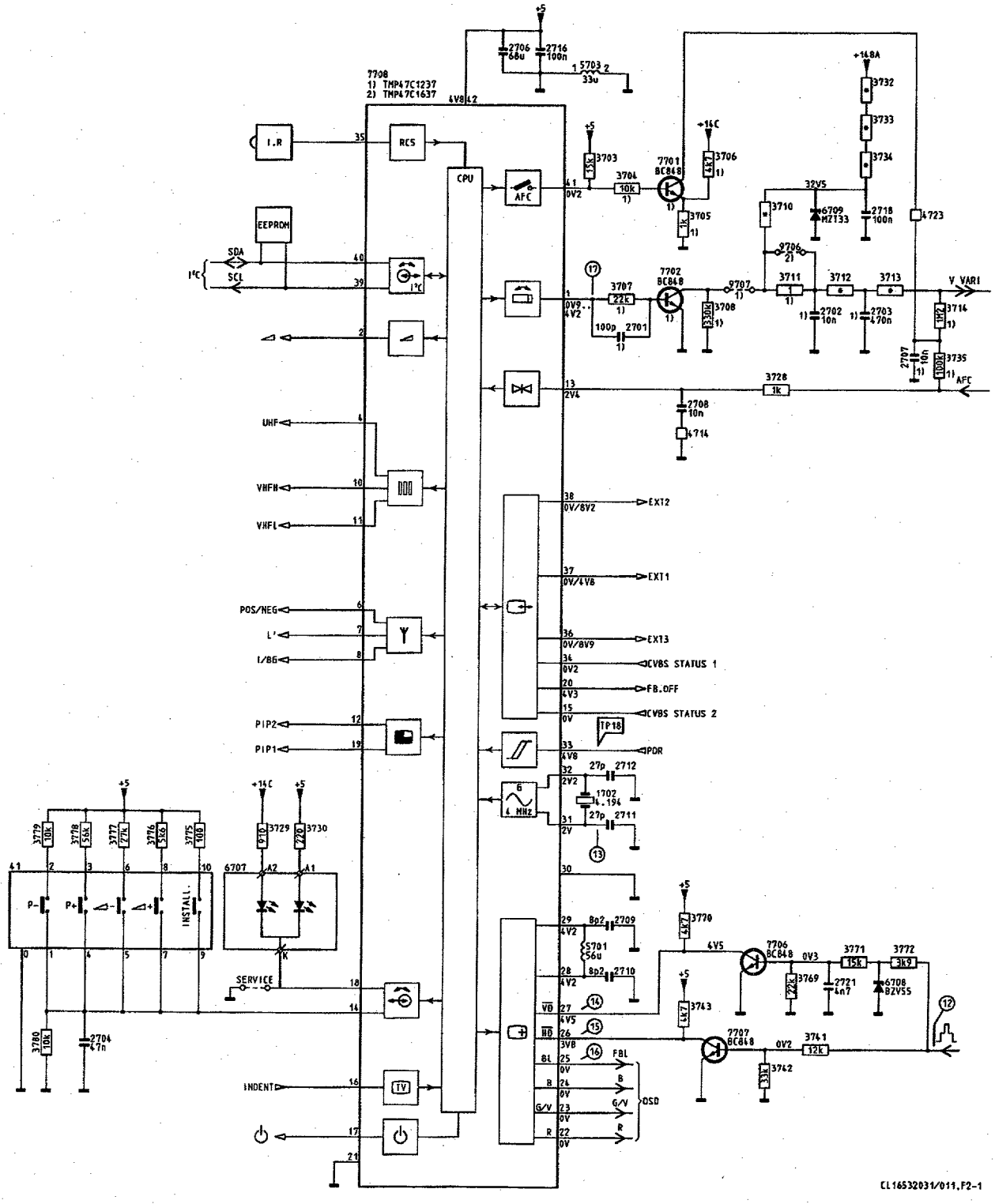
7708
1) TMP47C1237
2) TMP47C1637
CPU
EEPROM
I.R
RCS
AFC
I²C
SDA
SCL
UHF
VHFH
VHFL
POS/NEG
L'
I/BG
PIP2
PIP1
INDENT
SERVICE
EXT2
EXT1
EXT3
CVBS STATUS 1
FB.OFF
CVBS STATUS 2
PDR
TP18
6 MHz
V VARI
AFC
FBL
OSD
INSTALL.
CL16532031/011.F2-1

Fig. 2.1

the outputs of switches 7312-2A and 7312-2B, respectively.

## PIP source selection

Via switch 7801-3A a choice is made between CVBS from the IF and CVBS from EXT2, which is composed by adding the separated Y and C signals.
Switch 7801-3B chooses between CVBS from EXT1 and CVBS from EXT3. Finally, switch 7801-3C selects one of these two groups of signals and feeds it to the PIP module.

## The luminance path

The luminance signal (Y) goes via a chroma rejection filter, which will be short-circuited via 7303 if the signals originate from EXT2, and a delay line in IC7308, to video control IC7309. The Y-signal is also presented to teletext decoder 1003 and to sync separator IC7470.

## The chrominance path

The chrominance signal goes via a chroma band-pass filter to chroma decoder IC7305/7306. The chroma decoder produces demodulated colour difference signals (U and V), which are sent to base band delay lines IC7307 for phase correction. The corrected U and V signals are then routed to the CTI section of IC7308 and from there to video control IC7309.

## Video controle and RGB output amplifiers

In the video control the YUV signals are converted into RGB signals. These signals are fed to a selector switch, with which RGB originating from EXT1 and the PIP module can be blended in. RGB from the teletext decoder and On Screen Display (OSD) can be blended in via a second selector switch. After the composite RGB signals have been adjusted for colour saturation, brightness, contrast, picture tube cut-off points, white balance and peak-white limitation, they are fed to the RGB output amplifiers.
The RGB output amplifiers, which are located on the picture tube panel, drive the picture tube.

## The sound path

Four sound sources are presented to the sound path. Sound from the tuner is demodulated and decoded into low-frequency sound on the IF/sound module. This LF signal (internal sound) is also output on euroconnectors EXT1 and EXT3.
From the external connections EXT1, EXT2 and EXT3, LF sound is input, which is selected with switches 7802-2B and 7312. Then a choice is made between external and internal sound, which is then routed further through the sound control and finally reaches the sound output amplifier.
There are three basic versions for the IF/sound modules: mono, stereo and NICAM.

## The sync separator and the line and frame circuits

The Y signal is presented to IC7470, where frame and line control pulses are generated in addition to the so-called sandcastle pulse. The frame circuit provides vertical deflection and the line circuit horizontal deflection. The line circuit also supplies the +200, +14, +8 and -26 supply voltages.

## Operation

The whole process is controlled from a single-chip microcomputer. The microcomputer communicates with the outside world via a menu-controlled operating system. The microcomputer is responsible for tuning the channel selector and for setting the various controls and switches.

## Power Supply

The mains-isolated power supply is of the SOPS type. The drive circuit for the switching transistor and the regulating section of the power supply are integrated in two IC's. The power supply provides the +148, +16, -16, +32 and +5 supply voltages.

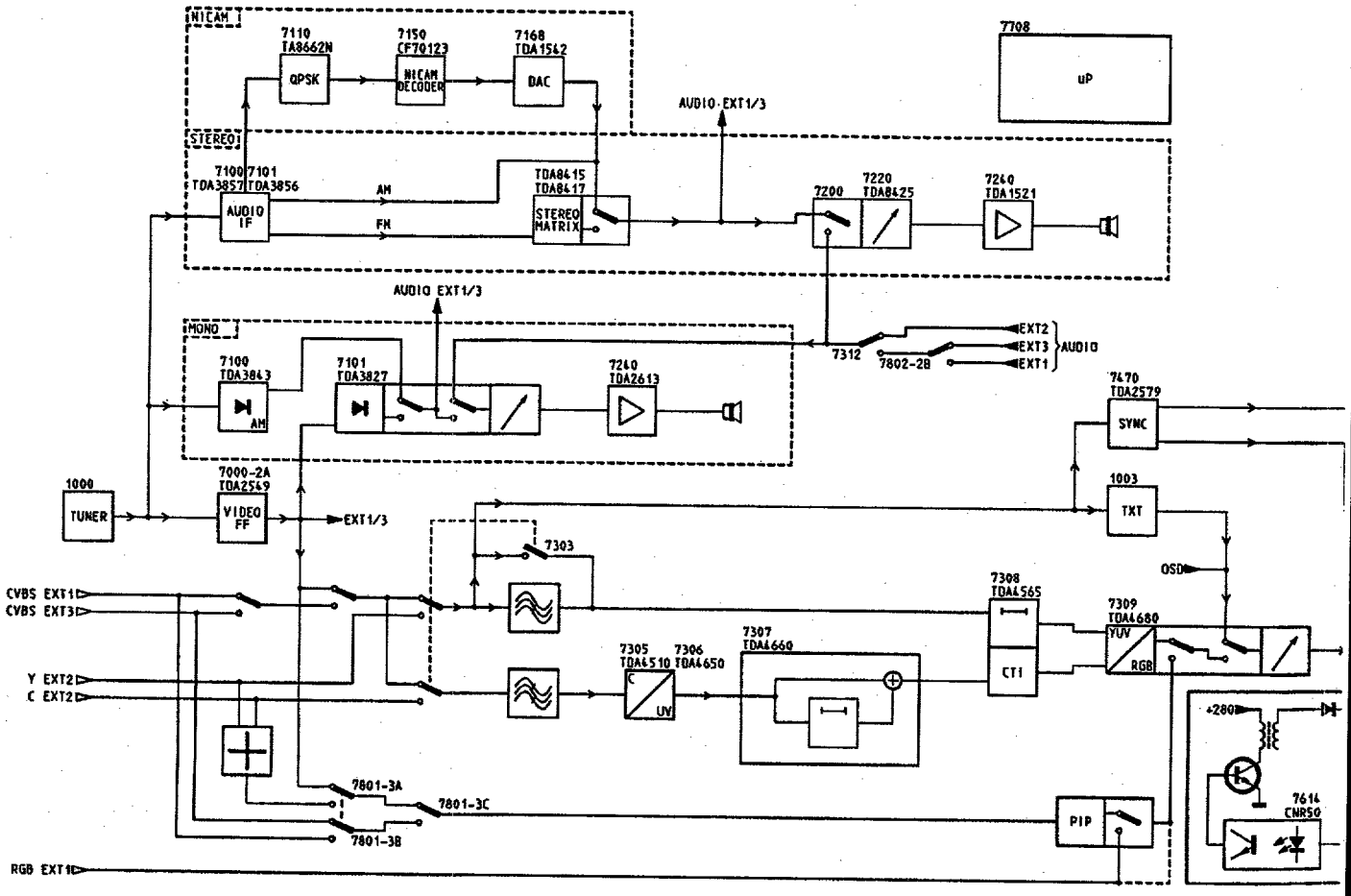


Fig. 1.1

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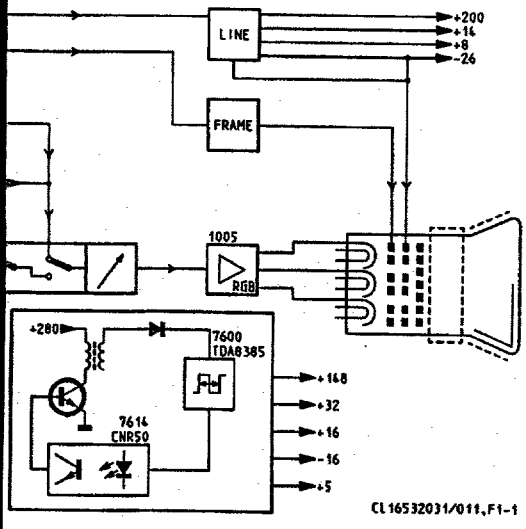

## Service Default Mode

When the set is switched on with the mains switch, a Power On Reset (POR) will be generated on pin 33 and the microcomputer will be reset. After a reset, the microprocessor comes in an initialisation phase, in which the LED output (pin 18) is switched as input for a short duration, and the microprocessor can detect whether the service pins are short-circuited. If this is the case, the set will be brought in a defined state.

## Stand by

The power supply is switched into stand by via pin 17.

## External source selection

The external source is selected with switching voltages on pins 36, 37 and 38. The following signal sources may be selected: tuner, EXT1 (euroconnector 1), EXT 2 (Y/C connector) and EXT3 (euroconnector 2). If a source other than EXT 1 is manually selected, an RGB status signal present on EXT 1 will be blanked with the switching voltage on pin 20.
Table 2.4 gives the various levels on the pins in combination with the various external sources selected.
The CVBS STATUS signals originating from EXT1 and EXT3 are read on pins 34 and 15, respectively.

| SOURCE | PIN MICROCOMPUTER | | | |
|---|---|---|---|---|
| | 36 EXT3 | 37 EXT1 | 38 EXT2 | 20 FBOFF |
| TUNER | 0V | 0V | 0V | 0V6 |
| EXT1 | 8V5 | 5V | 0V | 0V |
| EXT2 | 8V5 | 5V | 8V | 0V6 |
| EXT3 | 0V | 5V | 0V | 0V6 |

Table 2.4

## On Screen Display

With the aid of the OSD generator, RGB information is generated which becomes available on pins 22, 23 and 24. An RGB switch in the video control is operated with the blanking signal on pin 25, so that the RGB information appears on the screen. Line and frame flyback pulses, with which the location on the screen can be determined, are applied via pins 26 and 27. An 8 MHz OSD-oscillator is connected to pins 28 and 29.

## Tuning

In GR2.1 two kinds of tuning systems are possible.
The VST tuning system is used in sets with microcomputer TMP47C1237 (mono sets) and the PLL tuning system in sets with microcomputer TMP47C1637 (stereo sets).

## VST tuning

With VST tuning, band switching of the tuner takes place by means of the band switching voltages on pins 4, 10 and 11. After amplification and smoothing, a pulse-width modulated signal on pin 1 supplies the Vvari voltage for the tuner. The AFC voltage originating from the IF module is measured on pin 13. This voltage is also fed back to the tuning voltage Vvari to compensate for the frequency drift of the tuner. During station search this feedback of the AFC voltage is disabled via pin 41. The IDENT input (pin 16) is for detecting when a station is found during station search.

## PLL tuning

With PLL tuning the band switching and tuning frequency data are sent via the I2C bus to the tuner. The AFC voltage is measured on pin 13. Pins 1, 4, 10, 11 and 41 are not used.

## Picture and sound adjustmemts

All picture adjustments take place via the I2C bus.
In stereo sets sound adjustments take place via the I2C bus.
In mono sets volume adjustment takes place via pin 2 of the microcomputer.

# 3. Tuner and intermediate frequency

Contents



## 3.1 The tuner

Depending on the system version of the unit, 4 different tuners can be used in the GR2.1 chassis (see fig. 3.1):

-- UV916 (for stereo units)
-- U944 (for stereo units for UK)
-- UV917 (for mono units)
-- U743 (for mono units for UK)

Stereo units have a PLL tuning system. The band switching and tuning take place via the $I^2C$ bus.
Mono units have a VST tuning system. The band switching takes place by means of the switching voltage at the pins 7, 8 and 10 of the tuner.

The tuning voltage Vvari is supplied via pin 11 in the case of mono units.

### Service tip

The tuning voltage can also be measured at pin 11 on stereo units.

The AGC (Automatic Gain Control) voltage is supplied via pin 5 for both mono and stereo units.
The intermediate frequency signal is present at the output of pin 17 of the tuner. This intermediate frequency signal is supplied to one of the following intermediate frequency/sound modules.

- Stereo intermediate frequency/sound module (STEREO module)
- Mono intermediate frequency/sound module (MONO module)
- NICAM intermediate frequency/sound module (NICAM module)

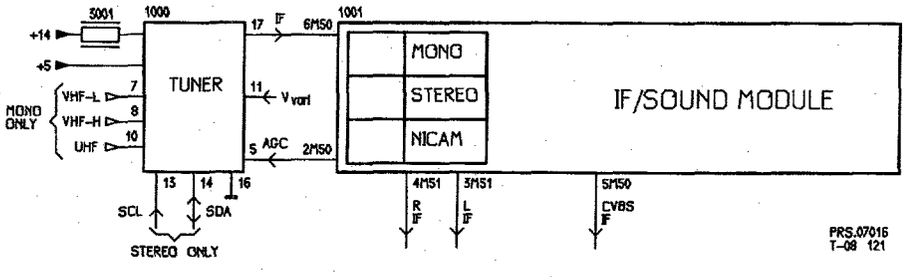


Fig. 3.1

# 3.2 IF signal path Stereo module

The intermediate frequency signal from the tuner is first supplied to a SAW filter (1010) (see fig. 3.2). The signal now splits into an intermediate frequency video signal "IF VIDEO" and a quasi split sound signal "QSS".
The "IF VIDEO" signal is supplied to pins 6 and 7 of the picture demodulator (TDA2549). The quasi split sound "QSS" signal is supplied to pins 23 and 24 of the TDA3856 in the case of multi units, and to pins 20 and 1 of the TDA3857 in the case of non-multi units.
For the SECAM L/L' systems (AM modulated sound) the intermediate frequency signal is supplied to pins 1 and 2 of the TDA3856 via a detunable bandpass filter. Using control signal L' the detunable filter is tuned to 32.4 MHz (SECAM L) or 39.9 MHz (SECAM L').

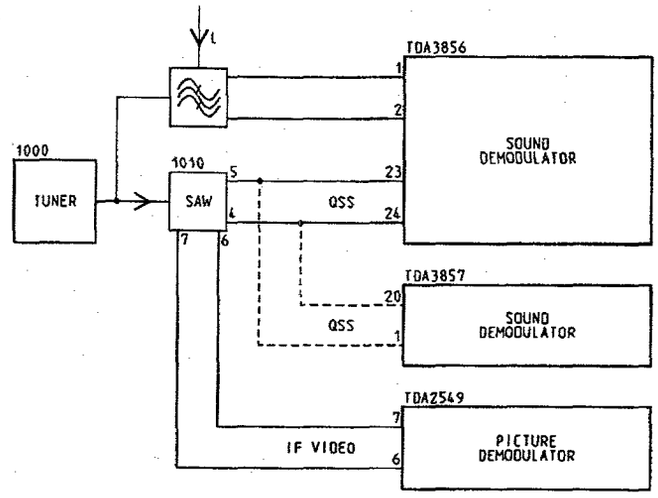


Fig. 3.2

## Intermediate frequency picture circuit (TDA2549)

The intermediate frequency video signal (IF VIDEO) is supplied to the TDA2549 (see fig 3.3). The amplification is determined by the IF-AVR circuit. After this amplifier, the signal is supplied to the video synchronous demodulator and the AFC demodulator. The video synchronous demodulator obtains its reference signal from a tuned circuit connected to pins 18 and 19 (tuned to 38.9 MHz). For multi units the circuit is tuned to 33.4 MHz using the control signal L' for SECAM L'.
After detection of the IF signal, the CVBS signal is present at pin 14. This signal is also supplied to a switch. Using this switch, a selection can be made between the internal video signal and a video signal supplied externally (CVBS EXT 1/3), after which one of the signals is supplied to pin 22 of the IC.
The AFC demodulator receives as the input signal the same signal as the video demodulator. The demodulation reference is determined by a circuit connected to pins 17 and 20. This circuit is tuned to 38.9 MHz and in the case of SECAM L' can be switched to 33.4 MHz using the control signal L'. A DC voltage of approximately 6V appears at pin 15 when a transmitter has been tuned correctly.
The moment when the delayed high-frequency AVR (RF AGC) starts to work can be adjusted using potentiometer 3016.

The IC is suitable for processing both positive (SECAM LL') and negative modulated signals (PAL/SECAM BG). Using a control signal POS/NEG, it is possible to switch between positive and negative modulated signals via pin 2.

## Intermediate frequency sound circuit (TDA3856/TDA3857)

The sound intermediate frequency demodulator TDA3856 is suitable for demodulation of both AM modulated and FM modulated signals (see fig. 3.4).
Selection between AM and FM sound takes place using the control signal (POS/NEG) at pin 5.

The mono FM (5.5 or 6.0 MHz) sound signal is at pin 15 of the TDA3856.
5.5 MHz or 6 MHz is selected using the control signal I/BG.
The stereo FM signal (5.74 MHz) is supplied again to the IC via pin 19. This stereo intermediate frequency sound signal is demodulated using the circuit at pins 6 and 7.
The mono FM signal (5.5 or 6.0 MHz ) is demodulated using a detunable circuit (at pins 18 and 11). The circuit is detuned between 5.5 and 6 MHz using the control signal I/BG.

Using the POS/NEG control signal, a selection is made between the AM sound signal (present at output pin 9) or the stereo sound signal (2R) plus the mono sound signal (R+L) sound (present at the output pins 8 or 9).

There is no AM sound path in the case of the TDA3857. The stereo signal (2R) is present at output pin 6, while the mono signal (R+L) is present at pin 7.

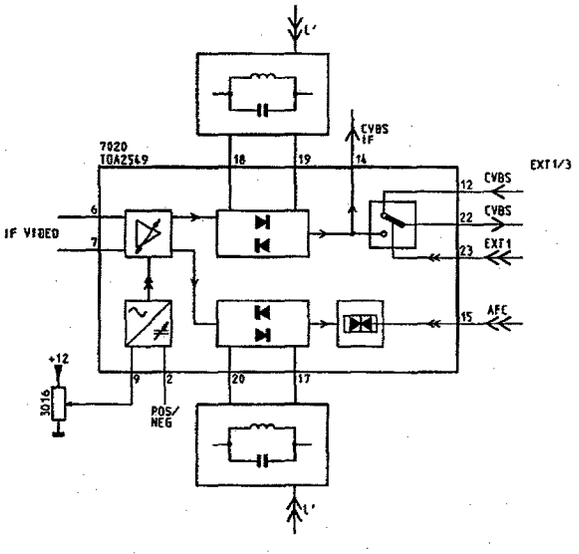


Fig. 3.3

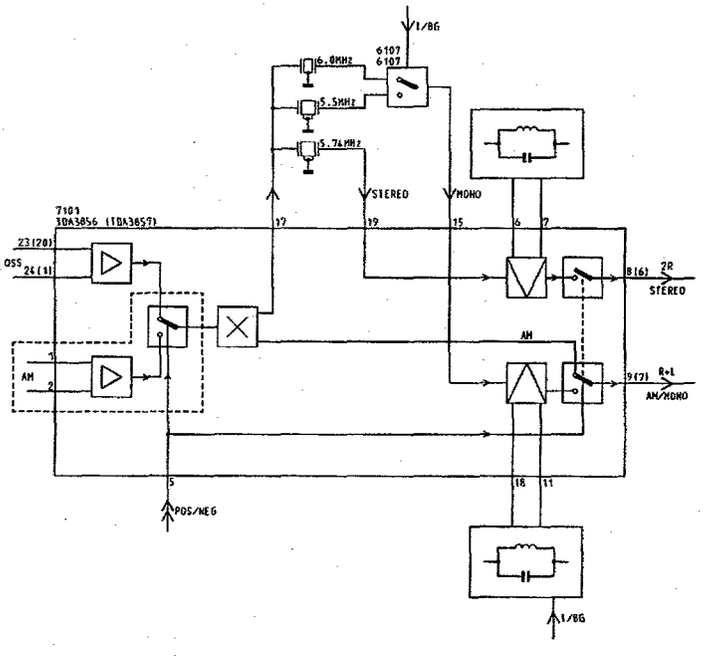


Fig. 3.4

# 3.3 IF signal path Mono module

The intermediate frequency signal from the tuner divides into an FM intermediate frequency sound and video path in the case of multi units (see fig. 3.5) and an AM intermediate frequency sound path (see fig 3.6). The AM intermediate frequency sound path is not present in the case of single system units.

## FM intermediate frequency sound and video path

The intermediate frequency signal is first sent to a detunable filter. In the case of negative modulation (PAL/SECAM BGI), this filter ensures that the bandpass is sufficiently large to 2enable intercarrier demodulation.
The filter may be narrower for positive modulation (SECAM LL') because demodulation is not intercarrier here.
The filter can be switched using the POS/NEG control signal.
The intermediate frequency video path is identical to that on the stereo module (see section 3.2).
FM modulated intercarrier sound from pin 1 of the demodulator IC7000 is supplied to pin 3 of the TDA3827 via the filter 1102 (1103 in the case of PAL I). In this IC the FM modulated sound is demodulated using a detunable demodulation circuit. The control signal BG/I detunes the demodulation circuit between 5.5 and 6.0 MHz.

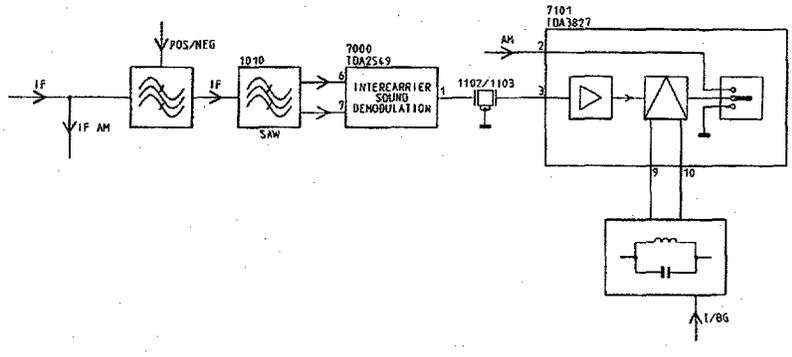


Fig. 3.5

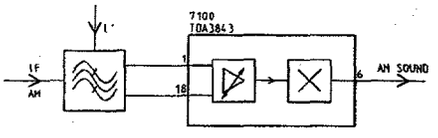


Fig. 3.6

## AM sound intermediate frequency circuit

The intermediate frequency signal is supplied to the AM demodulator TDA3843 via a detunable filter (see fig.3.6). The filter has a detunable characteristic because in the case of system L the sound is at 32.4 MHz and in the case of L' at 39.9 MHz. The filter is detuned using the control signal L'. The demodulated signal at pin 6 is supplied to the source selector switch in IC7101 (see section 4).

# 3.4 IF signal NICAM module

The signal processing is almost identical to that on the STEREO module, however the various circuits for multi-system reception are not present. For more data on the operation of the TDA3857 and TDA2549, see section 3.2.

# 4. The Sound path

Contents



## 4.1 Sound Stereo module

### The stereo decoder (TDA8417)

The two FM demodulated LF signals 2R and L+R are supplied to pins 7 and 8 of the stereo decoder TDA8417 (see fig. 4.1).
In the case of MULTI-system units, the low-frequency AM sound signal (L+R) is supplied to pin 9 of the stereo decoder via TS7104.
The status (MONO, TWO LANGUAGES or STEREO) is determined in the stereo decoder and, depending on the status, is set to the correct position by the microcomputer of the control, the dematrix circuit via the $I^2C$.
The low-frequency output signals R IF and L IF from the TV signal received (pins 11 and 12 of the stereo decoder) are supplied to the constant level output connector and to the euroconnectors EXT1 and EXT3.
In the case of single system units, an identification circuit ensures that the sound to the control amplifier can be interrupted via pin 18 (MUTE). This circuit is not present on Multi system units.
Using pin 19, the sound can be interrupted via the sound output amplifiers on the chassis.
The low-frequency output signals R and L (pins 13 and 14 of the stereo decoder) are supplied to the control amplifier.

### The control amplifier (TDA8425)

The sound source selected (the signals belonging to the status selected in the stereo decoder) is supplied to the control amplifier (IC7220, TDA8425).
In the control amplifier (see fig. 4.2) a selection is now made via the $I^2C$ bus between external sound (R EXT and L EXT) or sound from the stereo decoder.
In the control amplifier the functions BASS, TREBLE, VOLUME, BALANCE, SPATIAL, PSEUDO and the MONO/STEREO switch are also controlled via the $I^2C$ bus.
The set sound signals (pins 9 and 13) continue their way to the sound output amplifier on the chassis. However, the L signal is first rotated 180° in phase by TS7232; this gives control of a subwoofer, if present. The subwoofer is connected between L and R.
If L and R are supplied to the subwoofer, then no signal is transmitted in the case of mono (L and R equal). The subwoofer reproduces signals up to approximately 800 Hz.

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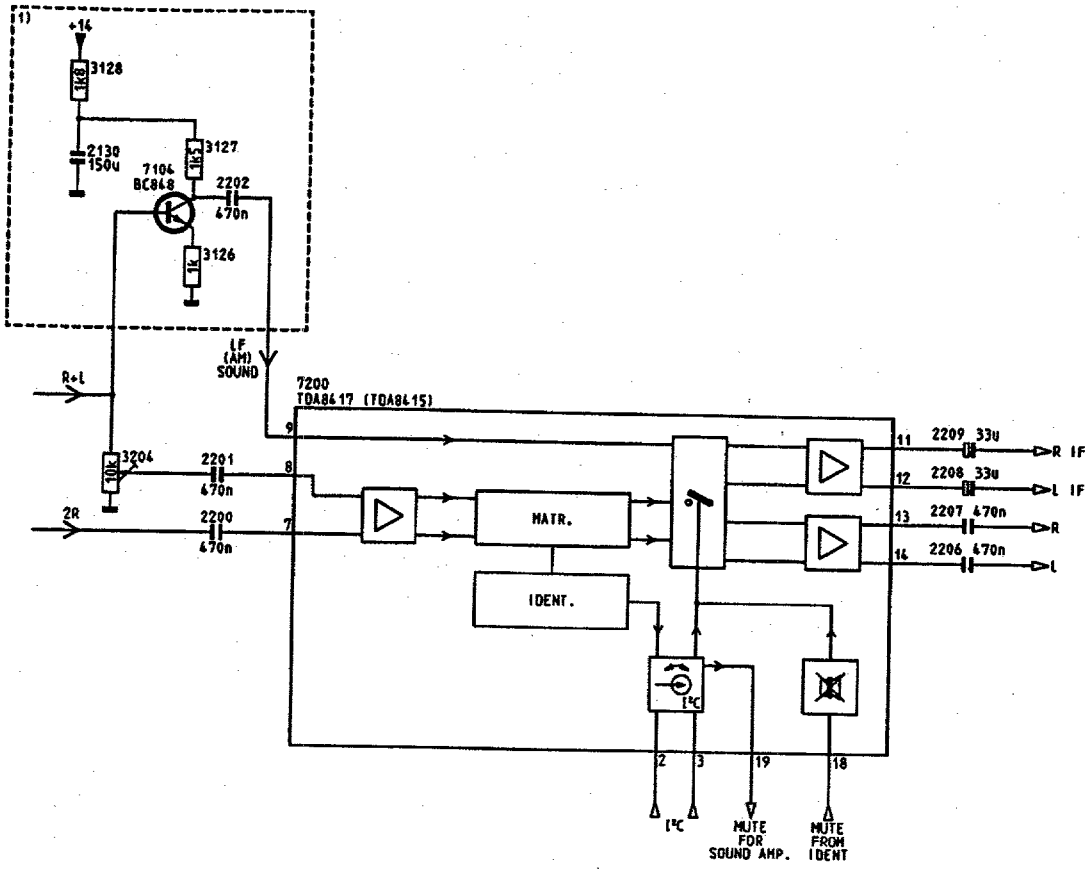


Fig. 4.1

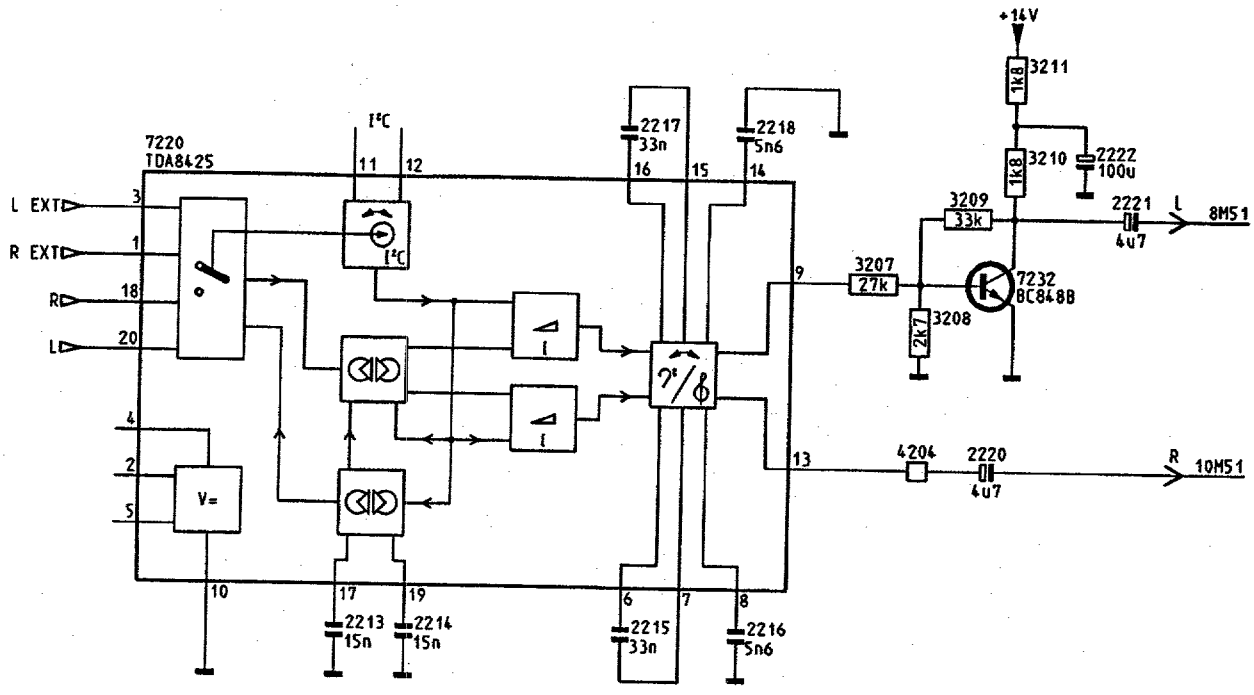


Fig. 4.2

# 4.2 Sound MONO module

The demodulated FM sound at pin 6 is supplied to the FM/AM/MUTE selector switch in the TDA3827 (if necessary with the AM modulated sound at pin 7) (see fig. 4.3). With the voltage level at pin 8 a selection can be made between MUTE, FM or AM sound.

Pin 8 has the following property (see table 4.1):

| Voltage level | Position of selector switch |
|---|---|
| < 0,9V | MUTE |
| 1,9..2,7V | FM |
| 4,7..5,6V | AM |

Table 4.1

**Source selection on MULTI-system units:**

With a SECAM L/L' signal (AM modulated sound and positive modulation), the POS/NEG control signal is "low". Consequently, TS7102 blocks so that the voltage at pin 8 is such that AM sound is selected.
With a PAL/SECAM BG or PAL I signal (FM modulated sound and negative modulation), the POS/NEG control signal is "high", and consequently FM sound is selected.
The MUTE facility is not used on multi-system units.

**Source selection on SINGLE-system units:**

If a CVBS signal is present at pin 14 of the TDA2549 (CVBS IF), then this is detected and TS7041 starts to conduct (see fig. 4.4). The voltage at pin 8 is now such that FM sound is selected. If no CVBS signal is received, TS7401 blocks and the sound is interrupted (MUTE).

The selected signal is supplied to the euroconnectors (EXT 1) and (EXT 3) via pin 13 of the TDA3827 (see fig. 4.3). The signal selected is also supplied to a second source selector switch in the TDA3827.

**External/Internal source selector switch**

Using this second source selector switch a choice can be made between external sound (R EXT and L EXT) or internal sound by means of control signal EXT1.

**Volume control:**

The output signal of the second source selector switch is sent to an adjustable amplifier where the volume can be adjusted with the voltage at pin 16.At minimum volume TS7103 starts conducting, thus the sound is interrupted via the output amplifiers on the chassis (MUTE).

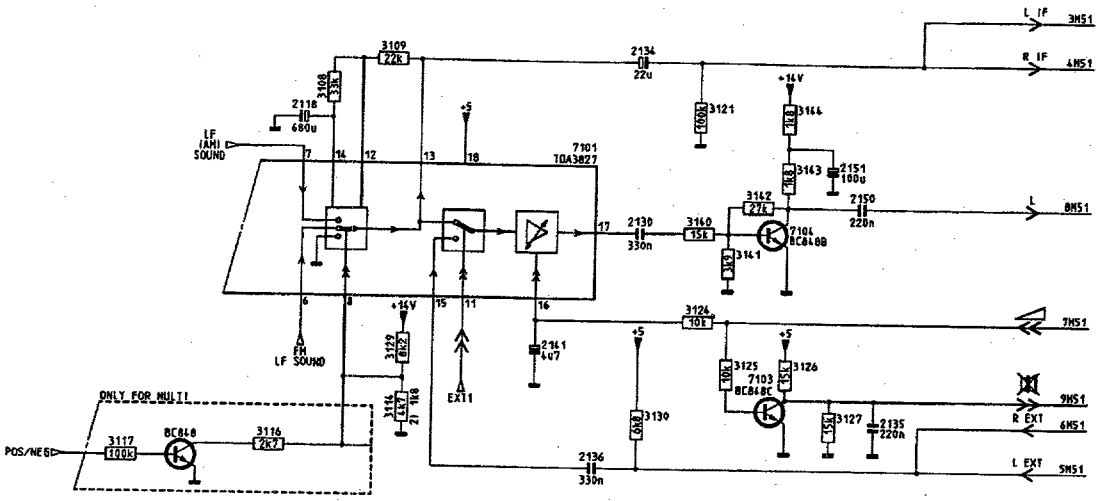


Fig 4.3

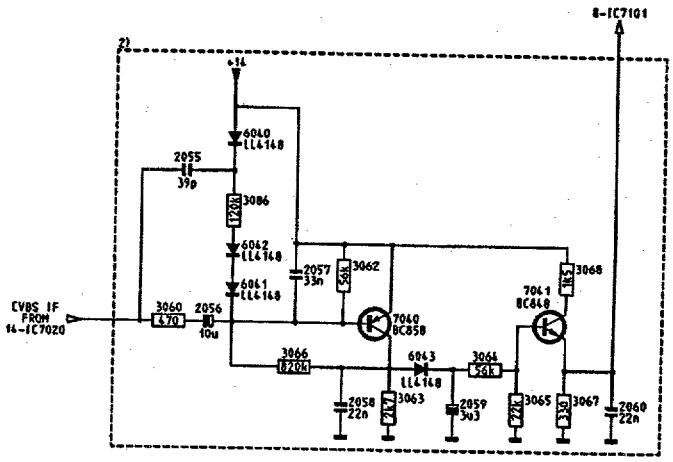


Fig. 4.4

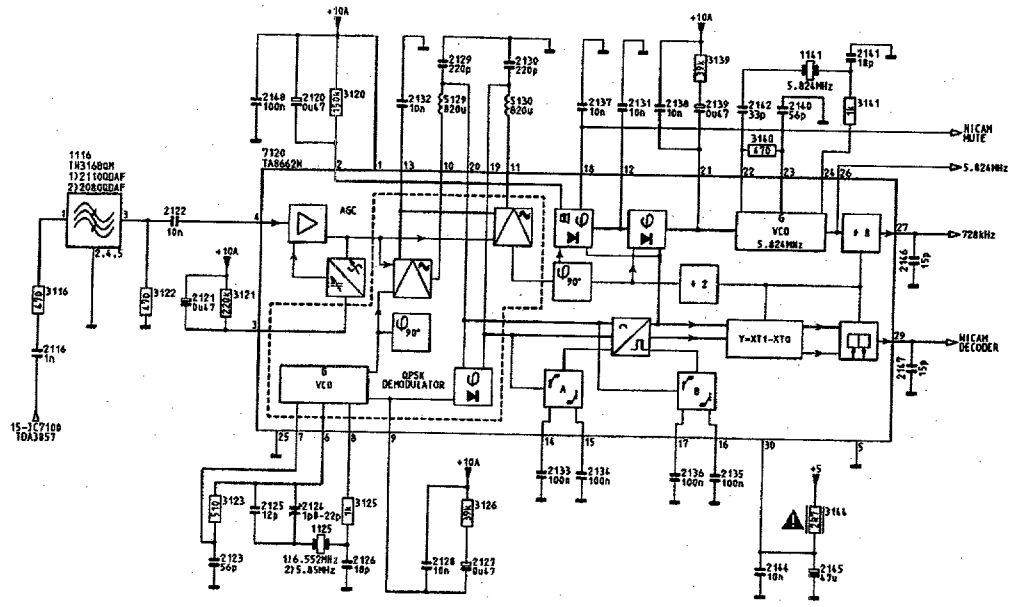


Fig. 4.5

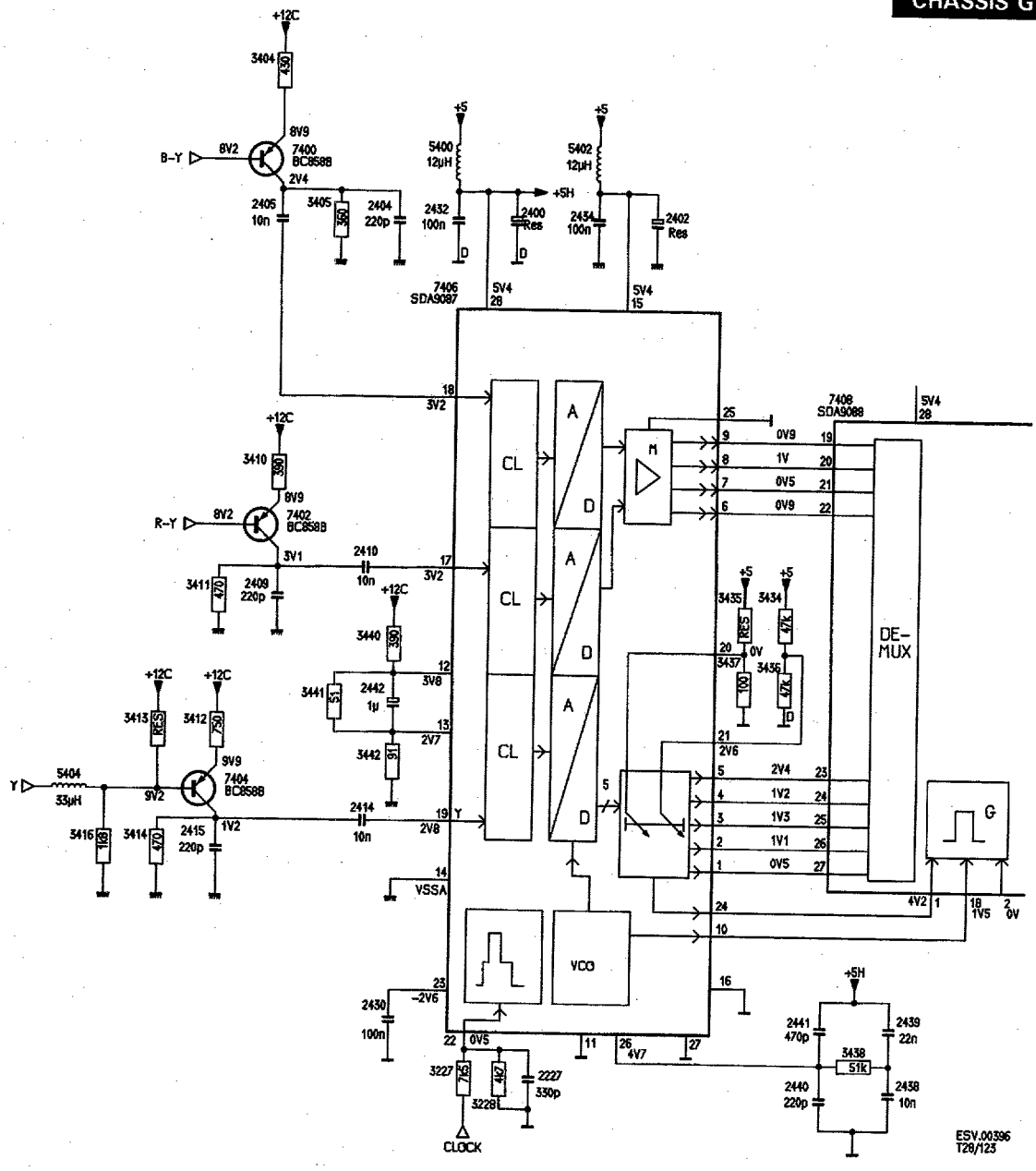
+12C
3404 430
8V9
B-Y
8V2
7400 BC858B
2V4
2405 10n
3405 360
2404 220p
+5
5400 12µH
2432 100n
+5H
2400 Res
5402 12µH
2434 100n
2402 Res
7406 SDA9087
5V4 28
5V4 15
18 3V2
CL
A
D
M
25
7408 SDA9088
5V4 28
9 0V9 19
8 1V 20
7 0V5 21
6 0V9 22
DE-MUX
3410 390
R-Y
7402 BC858B
3V1
2410 10n
17 3V2
3411 470
2409 220p
3435 RES
3434 47k
20 0V
3437 100
3436 47k
3440 390
12 3V8
3441 51
2442 1µ
13 2V7
3442 91
21 2V6
3413 RES
3412 750
9V9
7404 BC858B
Y
5404 33µH
9V2
3416 100
3414 470
2415 220p
1V2
2414 10n
19 Y 2V8
14 VSSA
5 2V4 23
4 1V2 24
3 1V3 25
2 1V1 26
1 0V5 27
G
4V2 1
18 1V5
2 0V
24
10
VCO
16
23 -2V6
2430 100n
22 0V5
11
26 4V7
27
3227 750
3228 470
2227 330p
CLOCK
+5H
2441 470p
2439 22n
3438 51k
2440 220p
2438 10n
ESV.00396
T28/123

Fig 8.6

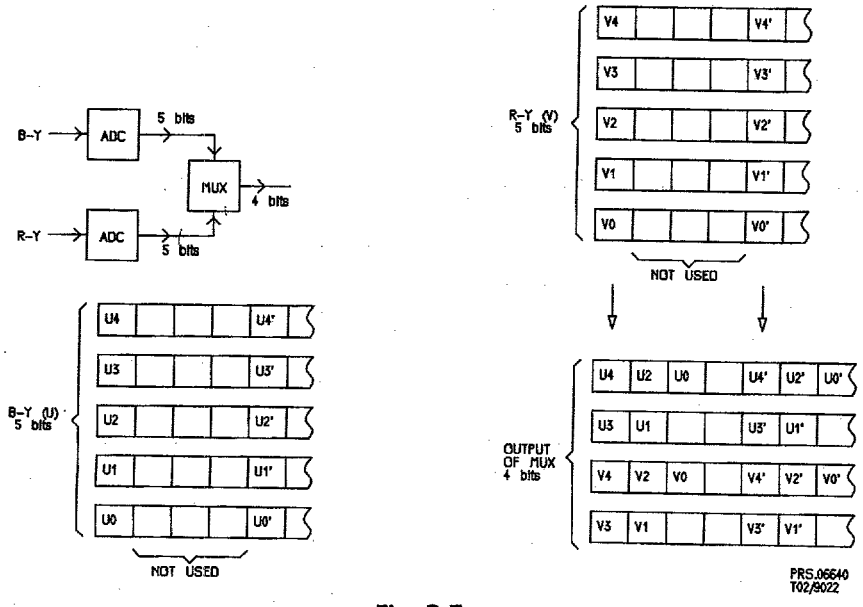
B-Y
ADC
5 bits
MUX
4 bits
R-Y
ADC
5 bits
B-Y (U) 5 bits
U4
U4'
U3
U3'
U2
U2'
U1
U1'
U0
U0'
NOT USED
R-Y (V) 5 bits
V4
V4'
V3
V3'
V2
V2'
V1
V1'
V0
V0'
NOT USED
OUTPUT OF MUX 4 bits
U4 U2 U0 U4' U2' U0'
U3 U1 U3' U1'
V4 V2 V0 V4' V2' V0'
V3 V1 V3' V1'
PRS.06640
T02/9022

Fig. 8.7

# 8.6 The PIP processor

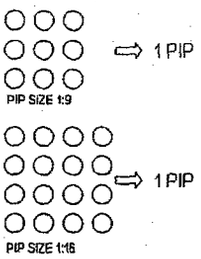


Fig. 8.8

The PIP processor receives one 5-bit Y and two 2-bits (U and V). These colour difference signals are demultiplexed first.

In order to place the PIP picture on a reduced format within the main picture, it must first be compressed. Depending on the PIP size selected, the average of 9 or 16 samples is determined in the decimation filter. This reduction always takes place with 3 or 4 samples in both the horizontal and vertical direction (see fig. 8.7).

In addition to this compression, several lines are left off on the top and bottom of the picture. A number of samples are also left off per line on the left and right. The remaining number of lines and samples is given in table 8.1.

| PIP SIZE | NUMBERS OF PIXELS PER LINE | | | NUMBER OF LINES |
|---|---|---|---|---|
| | | | | |
| 1/9 | 212 | 53 | 53 | 88 |
| 1/116 | 160 | 40 | 40 | 66 |

Table 8.1

Because the sample frequency for R-Y and B-Y is 4 times lower than for Y, the number of remaining pixels is also 4 times lower.

This reduced information is now stored in the memory using the INSET clock (see section 8.4).
The memory is read using the DISPLAY clock (see also section 8.4).
In order to convert the read-out Y, R-Y and B-Y signals into a matrix, R, G and B signals must have the same sample frequency. The interpolator fulfils this function.

### The interpolator

Three intermediate samples are always calculated and inserted in the interpolator by linear interpolation between two consecutive samples of R-Y and B-Y.
Y, R-Y and B-Y now have the same sample frequency (13.5 MHz).

In the PIP frame blanking part a pulse is produced which is high during the presence of the PIP picture. This fast blanking is carried out via pin 9 and is used to blank the main picture when the PIP picture is present.

### The RGB matrix

R-Y, B-Y and Y are converted into R, G and B in the matrix.

### The DA converter

In the digital-to-analog converter the digital R, G and B signals are converted into analog signals which are then carried out via pins 5, 6 and 7.

### EXT RGB / PIP RGB

In IC7380 a selection is made between RGB from EXT1 or RGB PIP using the PIP frame blanking signal.

# 9. Power supply

Contents



GR2.1 is fitted with an integrated SOPS (Self Oscillating Power Supply). A simple block diagram of the SOPS is shown in Fig. 9.1.

The SOPS is built up around two IC's: a special opto-coupler, CNR50 and the control IC, TDA8385.

The functions on the primary side include:
- undervoltage protection;
- switch-off circuit;
- start circuit.

The functions on the secondary side include:
- overvoltage protection;
- stand-by function;
- voltage control.

The switching period of the switching transistor TS can be divided into two main parts (see Fig. 9.2):
- Ton: the switching transistor is conducting
- Toff: the switching transistor is blocking current.

During Ton energy is stored in the transformer. During Toff this energy is passed on to the load. The turn-off moment of the switching transistor is controllable. To keep the turn-on losses to a minimum, the transistor is turned on at the moment the collector-emitter voltage is minimal.

The opto-coupler IC CNR50 provides the turn-off pulses for the switching transistor. After start-up, these turn-off pulses are generated by the LED in the opto-coupler which is driven by control IC TDA8385.

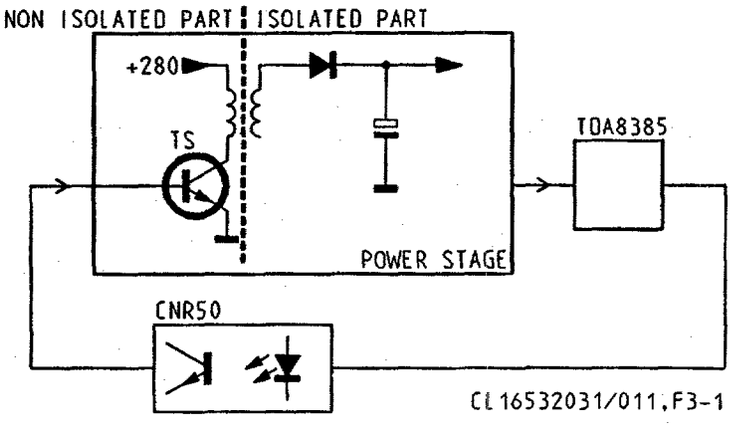


Fig. 9.1

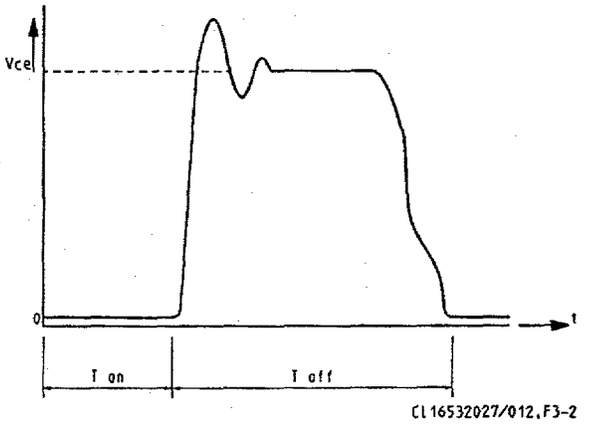


Fig. 9.2

# 9.1 The primary side

## Supply and initialisation of the CNR50

The CNR50 is powered via R3624 from the rectified mains voltage, and after start-up by transfer winding 6-19 of the SOPS transformer. Capacitor 2611 is charged via resistor 3624. Capacitor 2629 is charged via resistor 3625. If the voltage across capacitor 2611 (supply voltage of the CNR50) exceeds 14.8 V, and the voltage across capacitor 2629 is 2.95V, the CNR50 will start up. The opto-coupler will supply a starting current to the switching transistor to enable the supply circuit to start up. The supply of the opto-coupler is then taken over by winding 6-19.

## Undervoltage protection

After initialisation the voltage across capacitor 2629 is allowed to drop to 2.3 V. The voltage across capacitor 2611 (supply voltage of the CNR50) is allowed to vary between 3.9 V and 18V. If the supply voltage of the opto-coupler drops below 3.9 V, the supply circuit will be switched off by the opto-coupler. In this way it is prevented that control IC TDA8385 and the switching transistor are switched on at too low a supply voltage.

## Base drive circuits of hte switching transistor

When the switching transistor is conducting, the base drive current ib will be provided by winding 19-11. The output of the CNR50 (pin 6) causes the switching transistor to be turned off by means of the negative turn-off voltage Vref. This turn-off voltage is built up by means of the current i. This current consists of the sum of the base drive current, ib, and the supply current, iv, of the opto-coupler. Coil 5621 determines the size of the base drive current. R3620 and C2620 take care that the supply circuit can start up according to the blocking oscillator principle.
The negative turn-off voltage is determined by D6622, R3622, R3617, C2617 and D6617. L5619 determines the turn-off current.

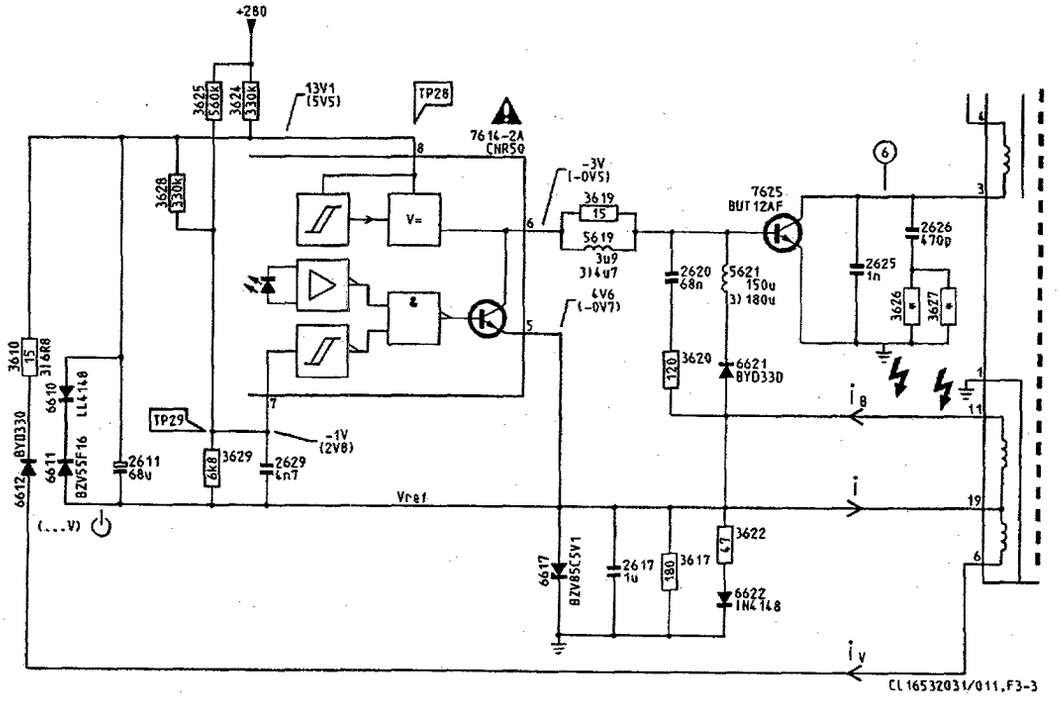


Fig. 9.3

## Vertical synchronisation

De vertical synchronisation pulses (V) come to the outside via point 3 and are sent to the PIP processor.

## Sandcastle generator

The line pulses supplied by the oscillator (G) go to the sandcastle generator via an amplifier.
The sandcastle pulse at point 17 has two levels:

- 12 volts during the line flyback
- 2.5 volts during the frame flyback

Because the PIP synchronisation does not control any line output stage, the supply voltage (point 10) and the start voltage (point 16) may be switched on at the same time.

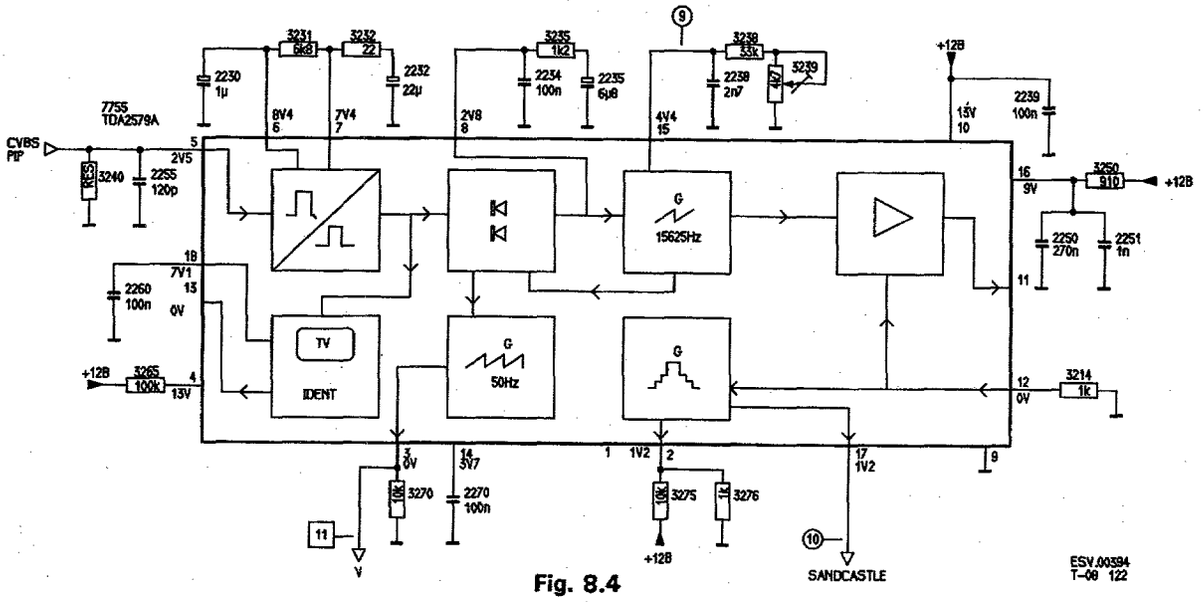


Fig. 8.4

## Display synchronisation IC (SDA9086)

The sandcastle of the main picture comes at point 8 of IC7410 via a differential amplifier (see fig. 8.5) and an emitter follower. This IC contains a VCO which shows 27 MHz. The clock (13.5 MHz) is produced by a PLL circuit which is synchronous with the sandcastle of the main picture and is present at pin 5. (At 50HZ the VCO is divided by 2.)
The horizontal synchronisation pulse (H) is derived from the clock (13.5 MHz/864) and is thus also synchronised with the sandcastle of the main picture.
The PLL compares the divided clock frequency with the signal at point 8 and emits up/down pulses which are smoothed by the RC network at pin 3. Using this the VCO is adjusted until the clock is precisely a multiple of the line frequency of the main picture.

The vertical synchronisation pulse from the field output stage ($V_{PIP}$) (see section 6.2) is sent to the PIP processor.

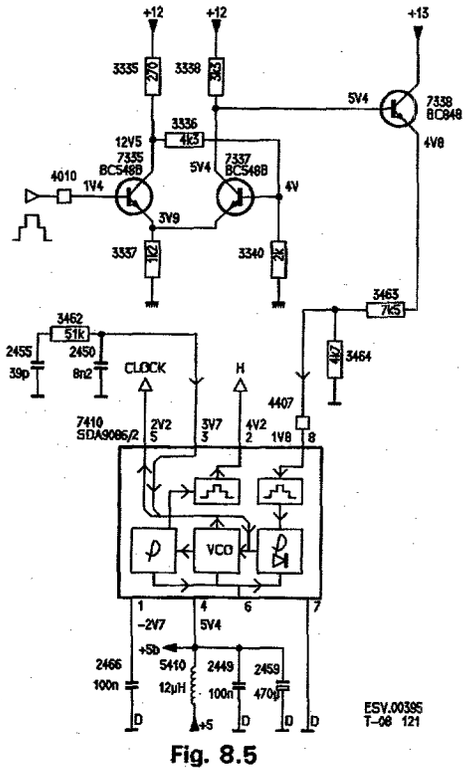


Fig. 8.5

## 8.5 De A/D converter

**Internal clock frequency**

The analog-to-digital converter is controlled by an internally produced 13.5 MHz clock frequency (see fig. 8.6). This clock frequency is locked to the clock signal supplied to pin 22 from the display sync IC7410.
The colour difference signals R-Y and B-Y enter the A/D converter via TS7402 and TS7400 via pins 17 and 18, respectively.

The Y signal first goes through a lowpass filter to filter out the chrominance signal and to prevent folding deformation.

**Reduced bandwidth**

Because the signal still ultimately appears in the PIP picture on the screen with a reduced bandwidth, the filter has a tilting point of only 1.3 MHz.

The reference voltages are determined in IC7406 by voltage dividers between pin 13 (Vref Low) and pin 12 (Vref High).

**Colour difference signals multiplexed**

Because the bandwidth of the R-Y signal and the B-Y signal is smaller than that of the Y-signal, the sample frequency for R-Y and B-Y may be lower than 13.5 MHz.
Thus, the colour difference signals are multiplexed from 5-bit signals with a sample frequency of 13.5 MHz to 2-bit signals with a sample frequency of 13.5 MHz. This takes place by using only one of each of the 4 samples and dividing the 5 bits of this sample over 2 bits and 4 clock periods (see fig. 8.6).
Because the signals are delayed by this (and by the later demultiplexing), the Y-signal must also be delayed.

**Luminance delay**

This extra delay takes place by an internal delay line, the delay of which is set by the voltage at pins 20 and 21. With the setting used the delay time is set at 6 clock periods.
A horizontal blanking pulse is obtained from the digital Y-signal, which is passed on to the PIP processor via pin 24, where this pulse is used to synchronise the read-in clock.

**Y: 5 bits**
**R-Y : 2 bits**
**B-Y : 2 bits**

The A.D.C. thus supplies a 5-bit Y-signal, a 2-bits B-Y signal and a 2-bit R-Y signal to the PIP processor.

# 8. PIP

## 8.1 Introduction

Contents



PIP is the abbreviation for Picture In Picture. This is a second picture, reduced, with limited picture sharpness, projected in the large picture. In order to look at another programme in this small picture, it is necessary to connect at least one other external source. The source which is made visible in the small picture gives no sound information. The sound information always comes from the large picture.

### PIP dimensions

A choice can be made between two formats of the PIP picture (1/9 or 1/16 of the main picture). Depending on this, the PIP picture contains more or fewer lines.

### PIP framework

There is a frame around the PIP picture. The frame thickness above and below is equal to 4 lines. The frame thickness on the left and right is equal to 0.5$\mu$s.

### Picture reduction

Only a limited part of the total video signal supplied is used for the PIP acquisition, namely 264 lines, and 47 $\mu$s of each line.
The picture is reduced linearly 3 times (4 times with large 1/16). This picture reduction is obtained by averaging picture lines and picture elements. See also section 8.6.

# 8.2 The block diagram

In the PIPSELECT part (A) it is determined which signal is shown in the PIP picture; this part is on the EURO module (see also section 5.2 Video source selection).

The PIP CVBS signal selected goes to the PIP panel. The CVBS signal is supplied here to the luminance-chrominance part (B) and to the synchronisation part (C). The chrominance signal is separated from the luminance signal and then demodulated, after which both the chrominance and the luminance signal are converted from analog to digital in the D/A converter (D).
Depending on the PIP size selected, the digitised signals are then reduced by a factor of 1:16 or 1:9 and stored in the memory of the PIP processor (E).

Because the second signal source is not synchronous with the main signal source, the signal processing described should by synchronous with the main picture. In order to achieve this, a separate synchronisation part (C) is added which supplies signals which are synchronised with the PIP input signal.

The digital Y, U and V signals stored in the memory are read out and converted to R, G and B signals. In order to obtain a stable PIP picture within the main picture, this must be read out synchronised with the synchronisation signals of the main picture. This synchronisation is obtained by controlling the PLL (F), which activates the read-out clock, with the horizontal synchronisation signal of the main picture.
A PIP fast-blanking signal (FBL PIP) is also controlled by the R, G, B signals if a signal is present from the PIP processor which produces switching between EXT RGB (from EXT1) and PIP RGB.
The RGB output signals, coming from the PIP module, are supplied to the IC7309 (see section 5.5).

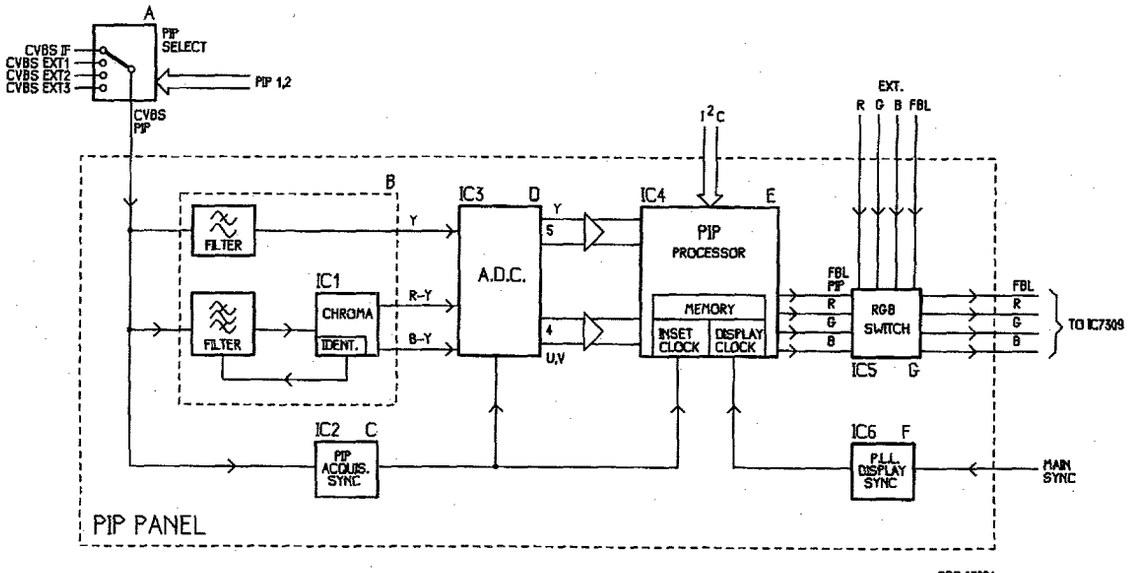


Fig. 8.1

PRS.07021 T28/125

# 8.3 PIP Chrominance/luminance path

The PIP-CVBS signal comes in on the basis of TS7234 (see fig. 8.2). The emitter signal branches off and goes to the PIP synchronisation IC (IC7755). The amplified signal present on the emitter of TS7233 is separated into a luminance and a chrominance signal.
The luminance signal goes to the ADC SDA9087 (IC7406) after a lowpass filter.
In the case of a single-system unit, the chrominance signal goes to the PAL decoder IC7126. In the case of multi-system units, the chrominance signal is sent to the multi-standard decoder IC7125.

## PAL only PIP

The chrominance signal is supplied to pin 9 of IC7126 (TDA4510) via a bandpass filter.
Colour demodulation takes place in this IC. For further information on the operation of this IC , see section 5.4.

## Multi-system PIP

In the case of multi-system PIP, the chrominance signal is supplied to pin 15 of IC7125 (TDA4554) via a bandpass filter. The filter can be switched and has 3 positions:

-SECAM In the SECAM position pins 25, 26 and 28 of IC7125 are low. The input filter now fulfils the circuit clock required for SECAM.

-PAL Pin 28 of IC7125 is now high, the filter is now tuned to 4.43 MHz.

-NTSC NTSC PIP is not used in chassis GR2.1.

## System identification

IC7125 (TDA4554) automatically switches one of the colour systems on and checks at the same time pins 25 to 28 for the switching of the input filter. The systems are recognised by the burst or identification signal on the back porch.
The identification recognises these signals and then makes one of the output points 25 to 28 high.
Pin 23 is earthed, which means that SECAM line identification is used.

The colour difference signals B-Y and R-Y from the demodulator (IC7125 or IC7126) are supplied to pins 18 and 17 of the A/D converter, respectively.

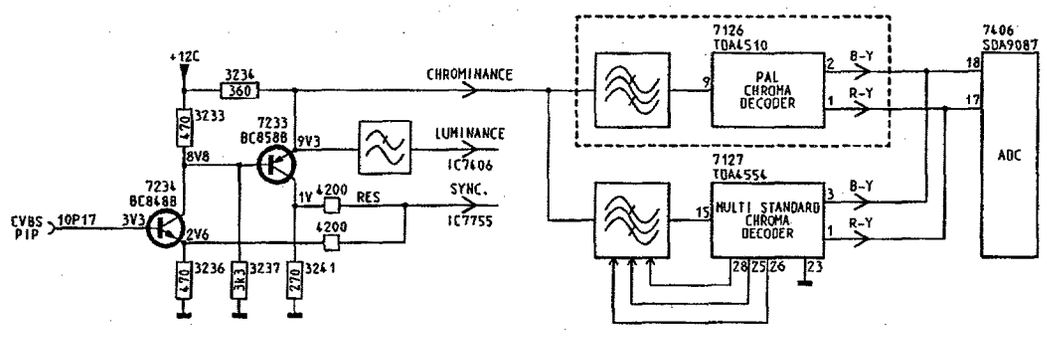


Fig. 8.2

# 8.4 PIP Synchronisation

Two synchronisations are necessary to process a PIP picture: (see fig. 8.3)

## Acquisition Synchronisation

After processing the PIP picture selected is stored in a memory in the PIP processor (IC7408). Synchronisation with the PIP picture is necessary for this. For this a separate synchronisation IC (TDA2579A) is used. This so-called acquisition synchronisation is used in:

- the chrominance part, where the burst key pulse is used to separate burst and chrominance;
- the analog-to-digital converter (A.D.C.), where the burst key is used for clamping, and where a 13.5 MHz clock is produced which is synchronised with the burst key pulse;
- the PIP processor, where the READIN clock is activated which is controlled by the horizontal synchronisation and the 13.5 MHz clock of the A.D.C. and by the vertical synchronisation pulses from the acquisition sync. IC.

## Display synchronisation

The display of the PIP on the screen must be synchronised with the main picture. The signals for the reading out of the memory of the PIP processor are therefore synchronised with the horizontal and vertical synchronisation pulses of the main picture (display sync).

## Aquisition synchronisation IC (TDA2579)

The CVBS PIP comes in at point 5 of IC7755 (see fig. 8.4). The horizontal oscillator is built up around the C2238, R3238 and R3239 connected to pin 15. Capacitor C2238 is charged with a constant current from the IC7755 to 6 volts and then discharged via R3238 and R3239. By varying the value of R3239, the discharge time, and thus the frequency, can be varied. In order to set the free-running frequency, the input signal can be short-circuited at point 5. The oscillator is now free and this frequency can be adjusted until the picture is still with R3239.

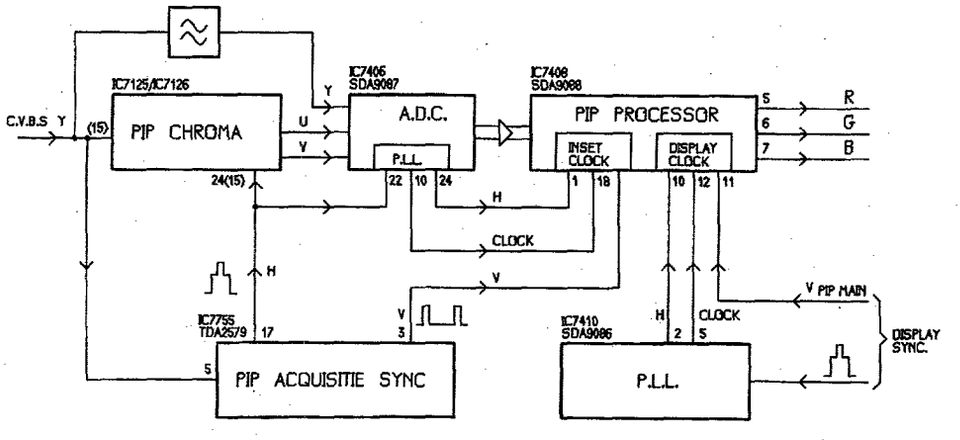


Fig. 8.3

PRS.07022
T28/123

# 6 Synchronisation and deflection

Contents



## 6.1 The block diagram

The complete line and frame synchronisation take place in IC7470 (TDA2579) (see fig. 6.1).
The frame output amplifier is built up around the transistors 7500, 7502 and 7503, and is powered by the +32V from the SOPS. The line output stage is built up around T5545 and is controlled via the transistors 7540 and 7545/7546. The line output stage is powered from the +148V coming from the SOPS.

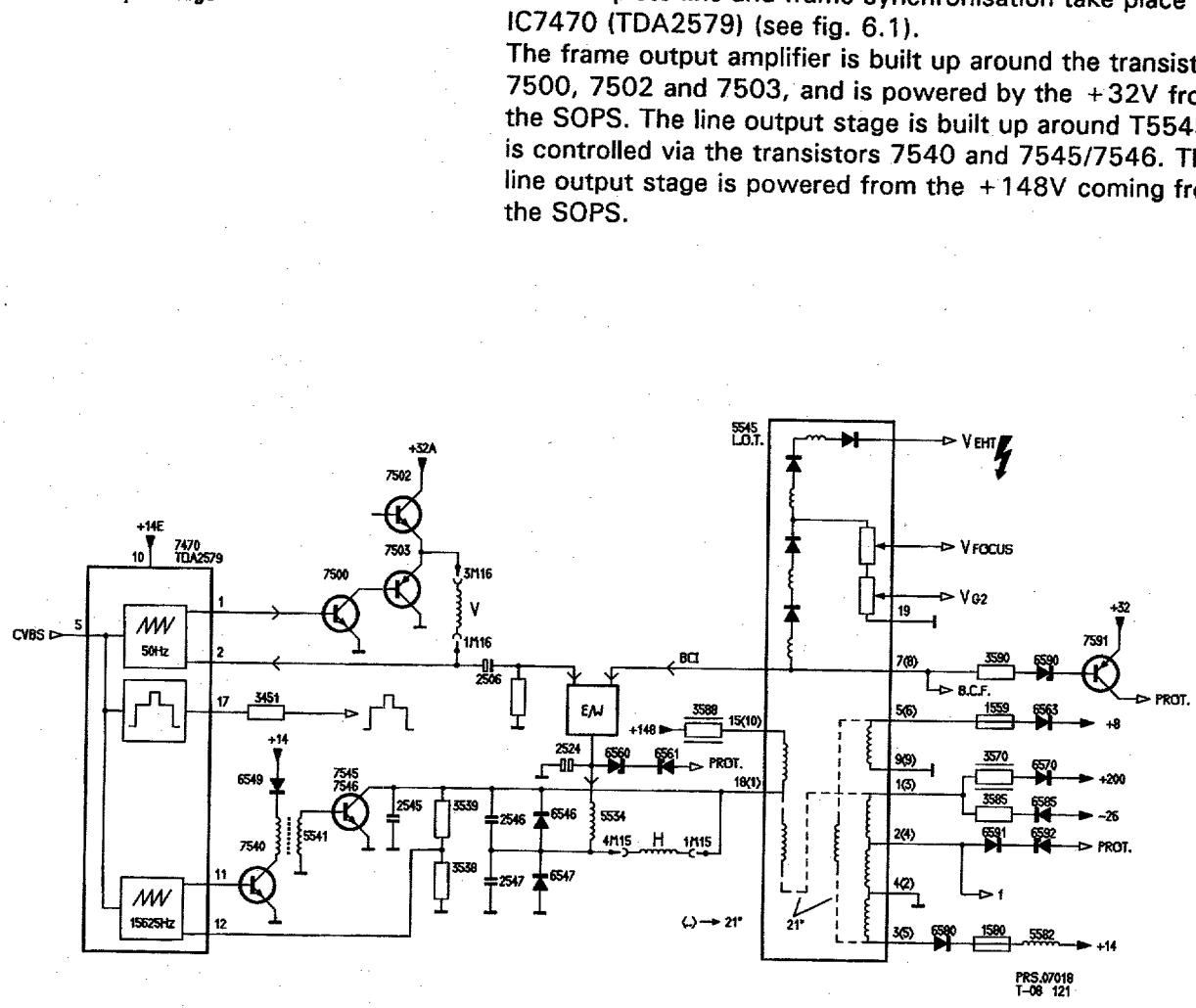


Fig. 6.1

## 6.2 Synchronisation

### Starting up

The starting up of the sync44hronisation IC (TDA2579) takes place in two phases (see fig. 6.2).
With the +32 supply voltage only the horizontal oscillator is started via pin 16 after the unit is switched on. The +14E supply voltage from the line circuit then provides the power supply of the other internal circuits via pin 10.
Consequently, the line output stage will start up gradually after the unit has been switched on.

### Synchronisation separator

Via pin 5 the CVBS signal arrives at the synchronisation separator. This detects the sync-top and black level and stores them in C2468 and C2469, pins 6 and 7,respectively.

## Time constants

The synchronisation can operate with 3 different control speeds depending on the size of the CVBS signal supplied to pin 5. Pin 18 indicates which time constant is switched on.

| Pin 5 | Pin 18 | Time constant |
|---|---|---|
| No signal | ≈ 1,2V | Small |
| Good signal | ≈ 6,2V | Normal |
| Signal < 0,7V | ≈ 10V | Large |

Table 6.1

## Line oscillator

The horizontal oscillator works by charging and discharging C2458 at pin 15. Using potentiometer R3457, the charging and discharging time can be adjusted and thus the oscillator frequency can be set.
The free-running frequency can be adjusted by short-circuiting the CVBS signal at pin 5 to earth and by stabilising the picture with R3457.

## The line output

The oscillator signal of the horizontal oscillator goes to the output of pin 11 for control of the line output stage via the line pulse phase comparator.
By varying the control voltage for the phase detector with R3461 (pin 14), the moment of the flyback can be adjusted. In this way, the picture can be centered horizontally with R3461.

## Phase comparator

As a result of the line output stage, a flyback pulse is formed which is taken to the phase comparator via pin 12. This uses it to adjust the phase of the outgoing line pulses.

## Sandcastle generator

The sandcastle pulse is at pin 17. This output signal has three levels:

1: 11V burst key
2: 4.5V line blanking
3: 2.5V raster blanking

## Picture tube protection

If the fed-back frame flyback voltage (FFB) from the frame deflection (supplied to pin 2) is greater than 1.9V or less than 0.5V, the sandcastle generator will increase the output (pin 17) to a minimum of 2.5V (raster blanking).
The sandcastle pulse is supplied to the following circuits:

- Via the EURO module to the PIP module (see section 8 PIP).
- The VIDEO circuits TDA4660, TDA4680 and TDA4510/TDA4650 (see section 5).
- The microprocessor for the reproduction of the OSD information.

## Vertical synchronisation

The vertical synchronisation is obtained from the horizontal synchronisation.
With the components between pin 4 and pin 3 the form is determined of the sawtooth control voltage for the frame output amplifiers.
This control voltage is used in combination with a flyback voltage "FFB" (pin 2) coming from the frame deflection in order to control the frame output amplifier via pin 1.

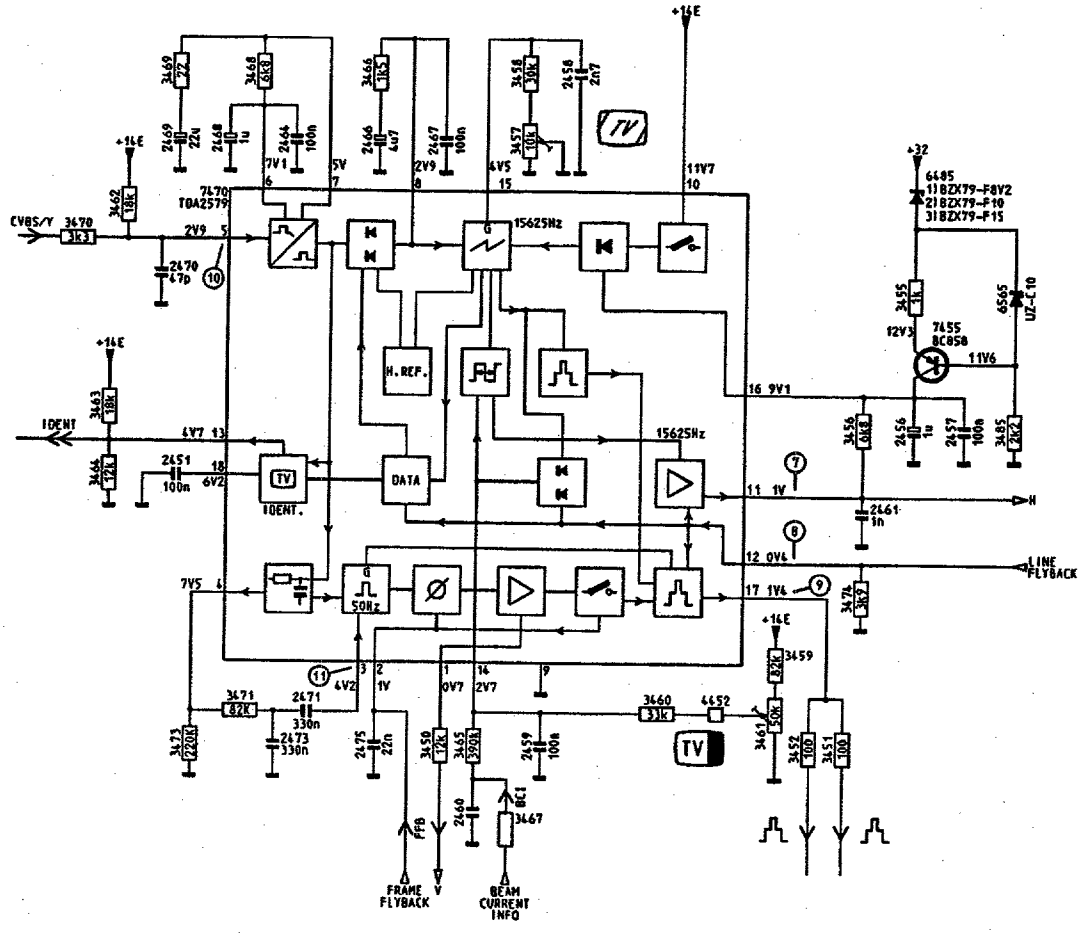
+16E
+32
CVBS/Y
IDENT
H.REF.
DATA
IDENT.
15625Hz
50Hz
TDA2579
7455 BC858
6485
1) BZX79-F8V2
2) BZX79-F10
3) BZX79-F15
LINE FLYBACK
FRAME FLYBACK
BEAM CURRENT INFO
TV

Fig. 6.2

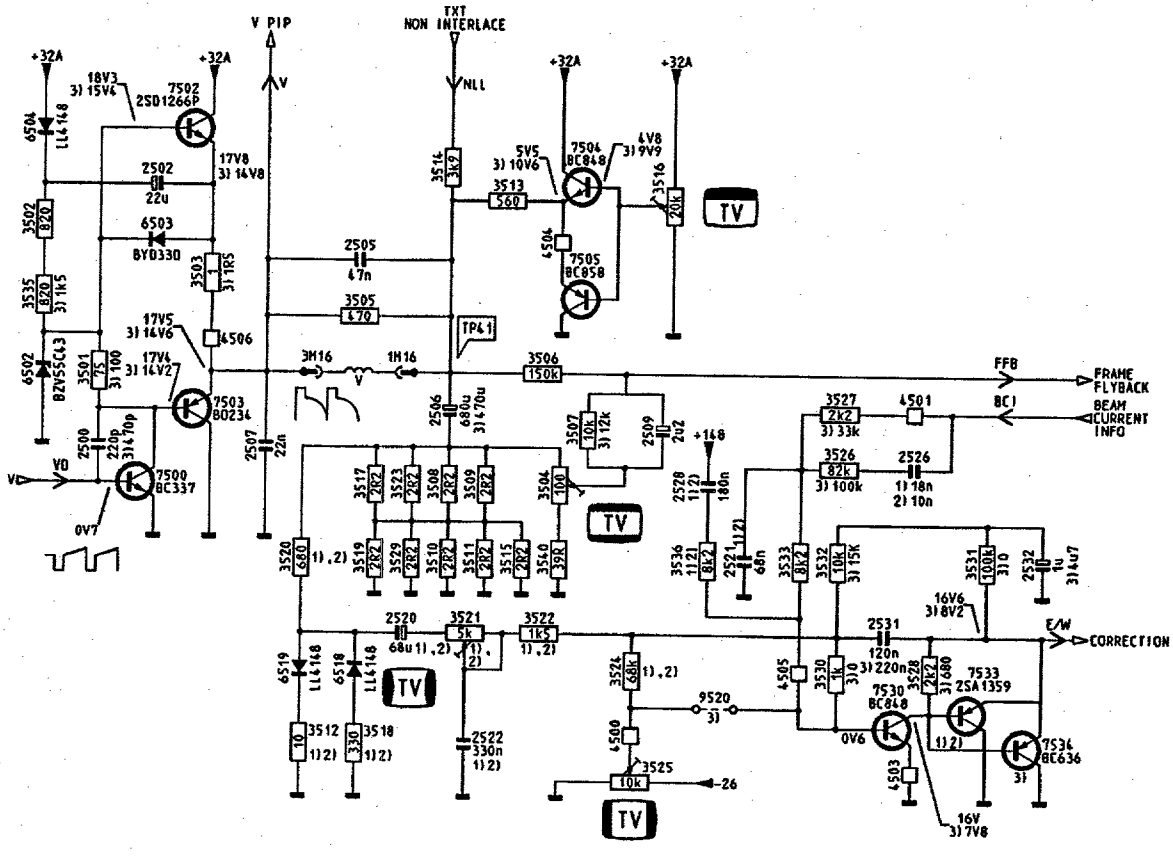
V PIP
TXT NON INTERLACE
+32A
7502 2SD1266P
7503 BD234
7500 BC337
7504 BC848
7505 BC858
6503 BYD330
6502 BZV55C4.3
TP41
FFB
FRAME FLYBACK
BEAM CURRENT INFO
E/W CORRECTION
7530 BC848
7533 2SA1359
7536 BC636
TV

Fig. 6.3

# 6.3 The frame output amplifier

The frame output amplifier (see fig. 6.3) supplies the required deflection current for the vertical deflection coil.
The control signal is supplied to the complementary balance amplifier formed by the transistors 7502 and 7503 via control transistor 7500.

## The flyback generator

The flyback generator is built up of discrete components and ensures that at the moment of the vertical flyback pulse the supply voltage is temporarily increased with the voltage which has built up during the trace time over C2502.
This temporary increase in voltage is required to obtain the required flyback time. In this way the supply voltage can remain low, which means that the dissipation is as low as possible.
Diode 6503 prevents the emitter base voltage of 7502 becoming too high during flyback.
The resistor 3505 which is located over the deflection coil and C2505 are used to damp the line frequency voltages in the vertical deflection coil, so that no interlacing faults occur.

The frame pulse V is supplied to the PIP module if present via the EURO module (see section 8 PIP).

The linearity and the amplitude of the deflection current are determined by the feedback to the synchronisation IC. This is realised as follows. The deflection current flows through, among other things, C2506, which produces a sawtooth voltage over potentiometer 3504, the amplitude of which depends on the deflection current.

## Picture height

Because with R3504 the amplitude of the frame flyback signal (FFB) is determined, the picture height is also set using this.

## S correction

A parabolic voltage is formed over C2506 by the sawtooth deflection current. A part of this is integrated, which results in an "S"-shaped voltage. This voltage is added to the fed-back sawtooth signal, which gives the S correction.

## Vertical position

The vertical position of the picture can be set using potentiometer 3516 by adding a direct voltage to the deflection coil.

## Teletext "Non-Interlace"

Because with Teletext reproduction no interlacing is required, the Non Interlace (NIL) signal is added.
The NIL signal is a 25 Hz block-shaped signal which ensures that the even and uneven frames fall over one another so that there is no interlacing.

### The east-west correction

Three voltages are supplied to the east-west correction circuit (consisting of TS7530, TS7533 and TS7534):

- The beam current information (BCI).
The size of the beam current is measured and supplied to the base of transistor 7530. This prevents the picture width varying with changing beam current.
- The required parabolic correction is obtained because a sawtooth voltage is supplied to the integrator TS7530, TS7533, TS7534 and C2531 via C2520, R3521 and R3522, which converts this into a parabolic shape.
The size of the east-west correction can be set using potentiometer 3521.
- A constant direct voltage.
This voltage can be set using potentiometer 3525, which is used to set the picture width.

## 6.4 The line output stage

The line pulses from pin 11 of synchronisation IC7470 are passed to switching transistor 7545/7546 (fig. 6.5) via control transistors 7540 and T5541. The deflection circuit consists of line deflection coil H, switching transistor TS7545/TS7546, and flyback capacitor 2545 and capacitor 2550.
The +148V supply voltages comes from the SOPS and is supplied to the line transformer.

### Output voltages

The following voltages are supplied by the line output transformer:
- EHT, Focus and VG2
- Beam current information (EHT info)
- The heater current for the picture tube (f)
- The supply voltages +8, +14, -26 and +200.

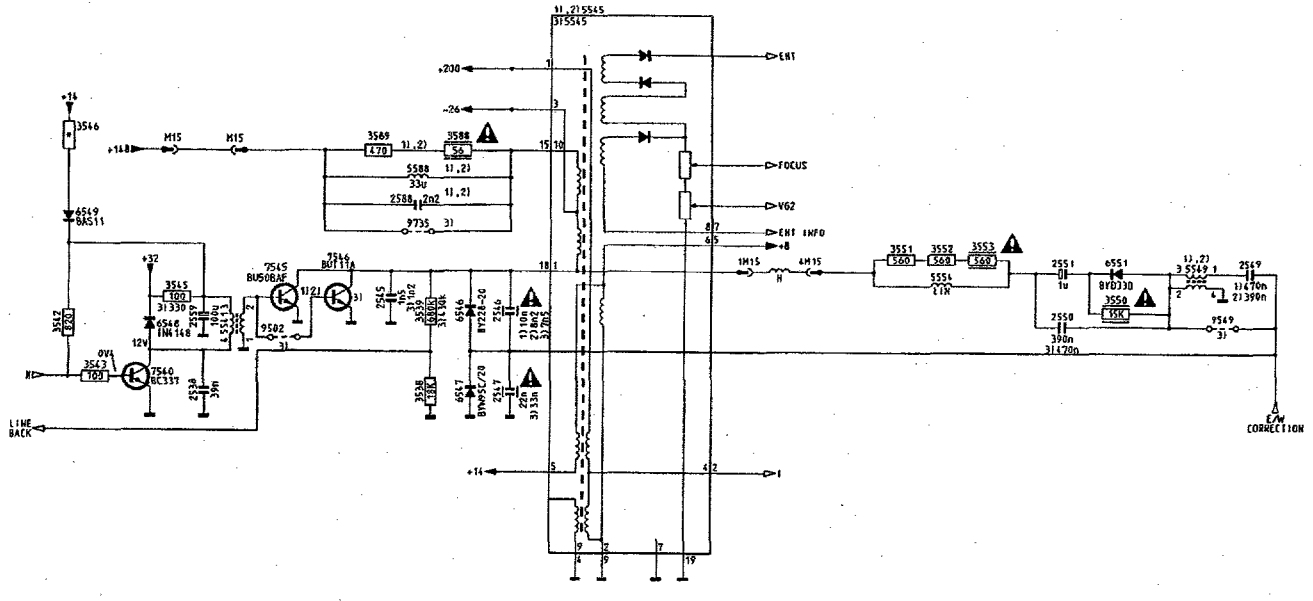


Fig. 6.4

# 7 Teletext

## Teletext interfacing

The connections of the teletext module (1003) are shown in fig. 7.1.
The teletext module is powered from the +8 and +14 supply voltages from the line output stage.
Communication between the microprocessor of the teletext module and the microprocessor of the chassis takes place via the $I^2C$ bus.
The transistors 7372 and 7374 prevent the $I^2C$ bus to the teletext module being blocked in stand-by. During stand-by both transistors block, which means that the $I^2C$ bus to the teletext module is made high impedance.

The CVBS/Y signal is supplied to the teletext module via transistor 7371. The level is modified for SECAM L' by means of the switching signal L'.
Together with the peak beam current limitation signal (PBCL) and the beam current limitation signal (BCL), the contrast signal at pin 8M18 determines the control signal that is sent to the contrast input of the video control IC7309.
The RGB output signals and the fast blanking signal (FBL) are sent to the video control IC7309 together with the OSD information from the microprocessor (see section 5.5).

The Non-Interlace signal (NIL) is supplied to the vertical deflection coil (see also section 6.3).

## The teletext module

For further information on the operation of the teletext module, see the diagram description Computer Controlled Teletext (CCT) published earlier.

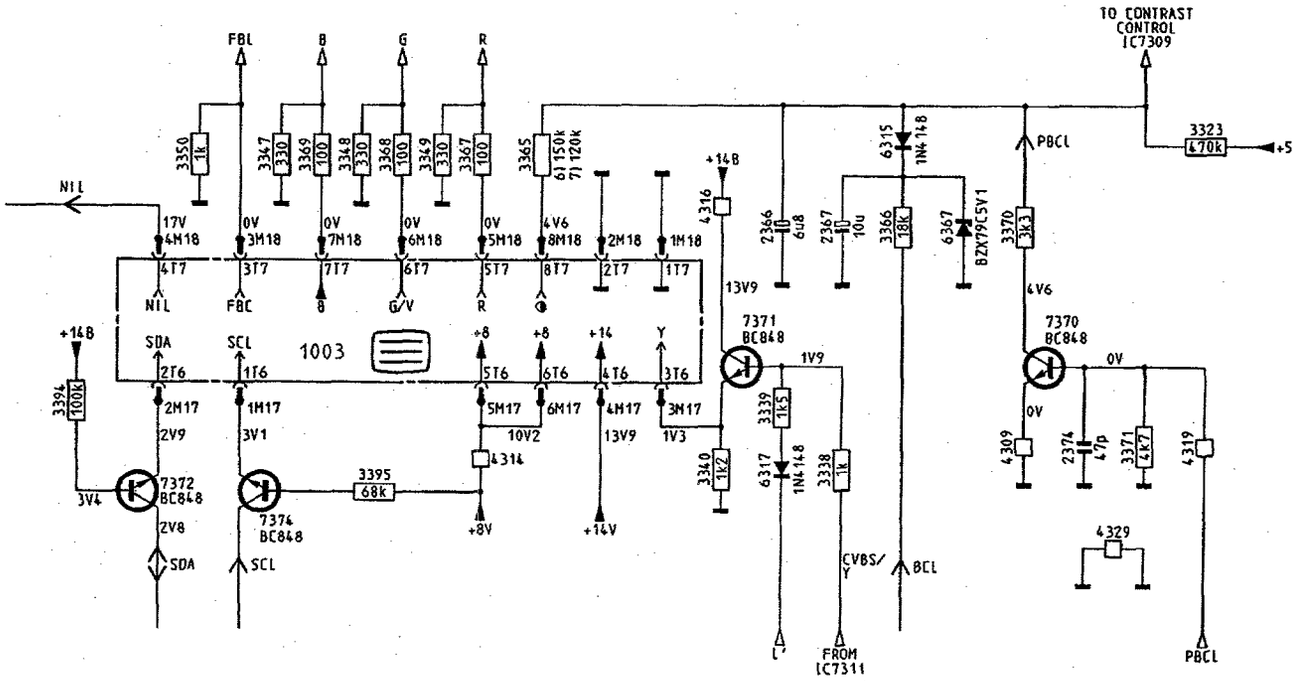


Fig. 7.1

# 5.4 The chrominance path

The CVBS/chroma signal is supplied to a chroma bandpass filter via TS7301 (see figs. 5.5 and 5.6). There are two possibilities: PAL chroma bandpass filter in the case of a PAL chroma decoder TDA4510 and a multi standard chroma bandpass filter in the case of a multi standard chroma decoder TDA4650.

**PAL chroma bandpass filter**

Together with C2301/C2303 and R3305, C2304 and L5301 form the filter. The whole of this circuit forms a bandpass filter tuned to 4.4 MHz.

**Multi chroma bandpass filter**

- PAL: In the case of a PAL signal, TS7302 starts to conduct. R3305 and C2305 now determine the tuning of the filter.
-SECAM TS7302 is blocked in the case of a SECAM signal. R3305 and C2305 are now not included in the circuit, which means that the filter is modified.

**Pal chroma decoder (TDA4510)**

The PAL chroma signal is supplied to pin 9 (TP19) of the TDA4510. This signal is demodulated and decoded to baseband B-Y and R-Y signals which are available at pins 2 and 1.

**Multi chroma decoder (TDA4650)**

The chroma signal (PAL or SECAM) is supplied at pin 15 (TP19) of the TDA4650. SECAM is recognised by the identification on the back porch of the CVBS signal.
The identification circuit in TDA4650 (IDENT) recognises these signals and in the case of SECAM makes pin 27 high. This switches the input filter.

The B-Y and R-Y signals from the chroma decoder (see fig. 5.1) are supplied to the baseband delay lines in the TDA4660 (IC7307). The direct signals and signals delayed a line time are added together.
The corrected B-Y and R-Y signals appear at pins 12 and 11 of the TDA4660.

**CTI (IC7308)**

In the R-Y and B-Y signal path the steep signal flanks, thus colour steps, are made even steeper. At places where there are no steep flanks in the colour difference signals, for example colour areas, the input signal signals are passed on to the output unchanged.

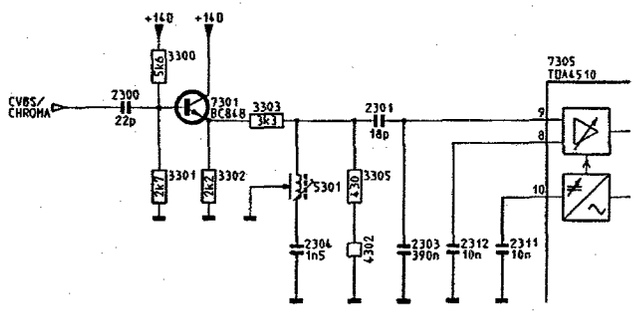


Fig. 5.5

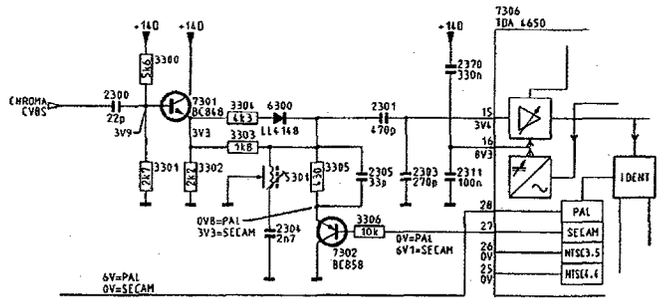


Fig. 5.6

# 5.5 The video control (TDA4680)

The video control (see fig. 5.7) has 3 input sources:

a. Y (TP8), R-Y (TP7) and B-Y (TP6) signals from the CTI IC7308.
b. R, G and B signals + blanking from the microprocessor (for OSD) and the teletext decoder if present.
c. R, G and B signals + blanking from euroconnector EXT1 or the PIP module if present.

Colour saturation, brightness and contrast can be controlled via the $I^2C$ bus for all these signals. There is also a beam-current limiter (PBCL) and a cut-off point stabilisation present (see § 5.6). The output signals are RGB signals which control the RGB output amplifiers on the picture tube panel.

If the voltage at pin 13 of the TDA4680 is low, the Y, R-Y and B-Y signals are passed to the control amplifiers. A high voltage at pin 13 switches the RGB signals from EXT1 or PIP to the control amplifiers.
A second switch is controlled with the OSD and/or TXT blanking signal. The TXT or OSD signals are switched through if pin 1 of the TDA4680 becomes high.

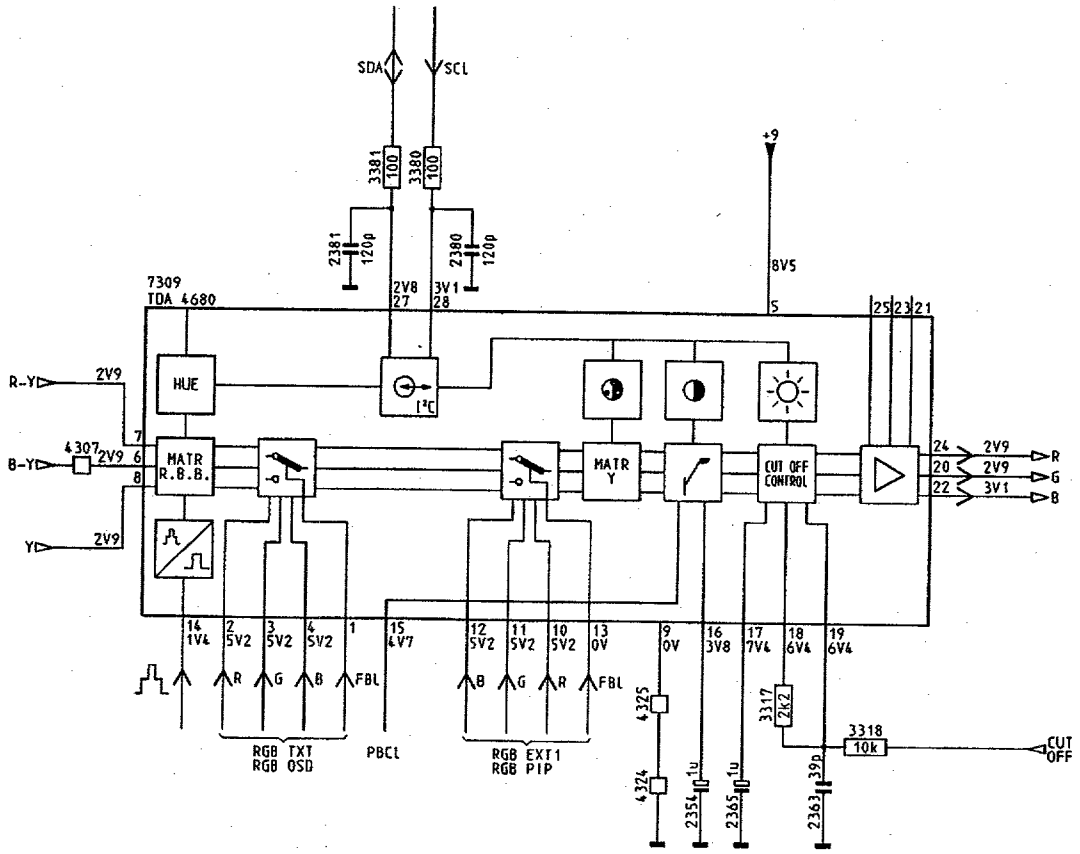


Fig 5.7

# 5.6 The RGB amplifiers

The RGB output amplifiers consist of 3 identical class A amplifiers built up around transistors TS7304, TS7305, TS7334, TS7335, TS7364 and TS7365.

## Peak beam-current limitation (PBCL)

The peak beam-current information is measured via D6301, D6331 and D6361, see fig. 5.8. If the voltage at one of the amplifiers is lower than approximately 43V (high beam current), then TS7391 will start to conduct, with the result that TS7370 will also start to conduct. Consequently, the voltage at pin 15 of the TDA4680 becomes lower and the peak white limiter becomes active. Peak white limitation is set using the service menu option WHITE BALANCE (C) (see fig. 5.10). The setting is made via the $I^2C$ bus.

## Cut-off point stabilisation

During the frame flyback a number of pulses are generated which enable the TDA4680 to set the cut-off points of the picture tube, see fig. 5.9. With the circuit formed by, among other components, R3313, R3343 and R3373, these pulses are measured and supplied to pins 18 and 19 of the TDA4680 via TS7421.
The cut-off points are set via the $I^2C$ bus using the service menu option CUT-OFF (see fig. 5.10).

## White balance

The white balance is also set via the $I^2C$ bus using the service menu option WHITE BALANCE (see fig. 5.10).

For more information on the service mode and the various options, see the service manual CHASSIS GR2.1.

## High voltage Focus VG2

The high voltage EHT, focus and VG2 voltages are supplied by the line transformer. The focus and VG2 can be set by means of potentiometers on the transformer L5545.

## Picture-tube flashover protection

In order to protect the receiver against picture-tube flashover, the following precautions have been taken:

1) spark gaps on all electrode connections on the picture-tube panel;

2) resistors in series with RGB electrodes (R3314, R3344 and R3374 (see fig. 5.8).

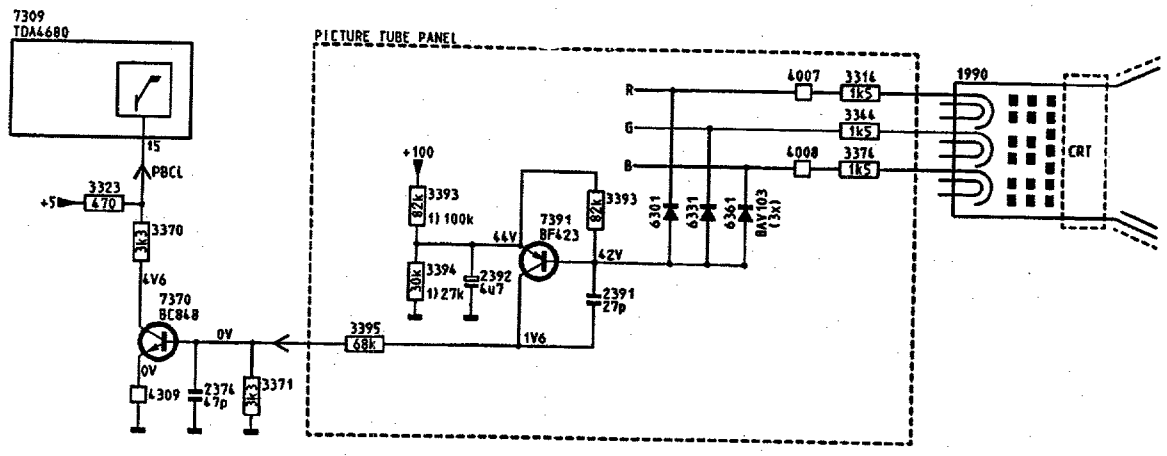


Fig. 5.8

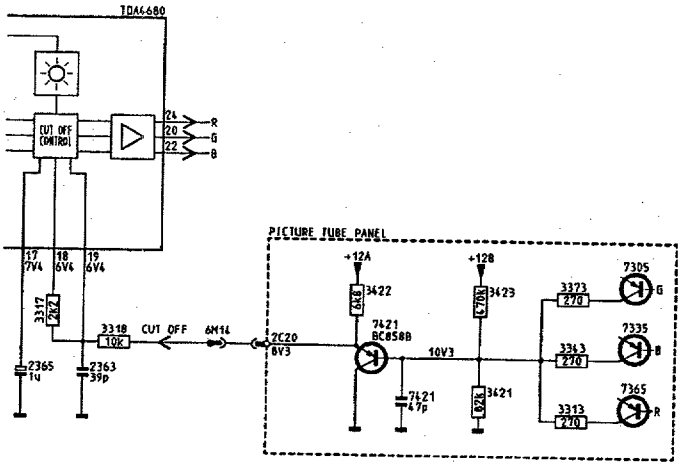


Fig. 5.9

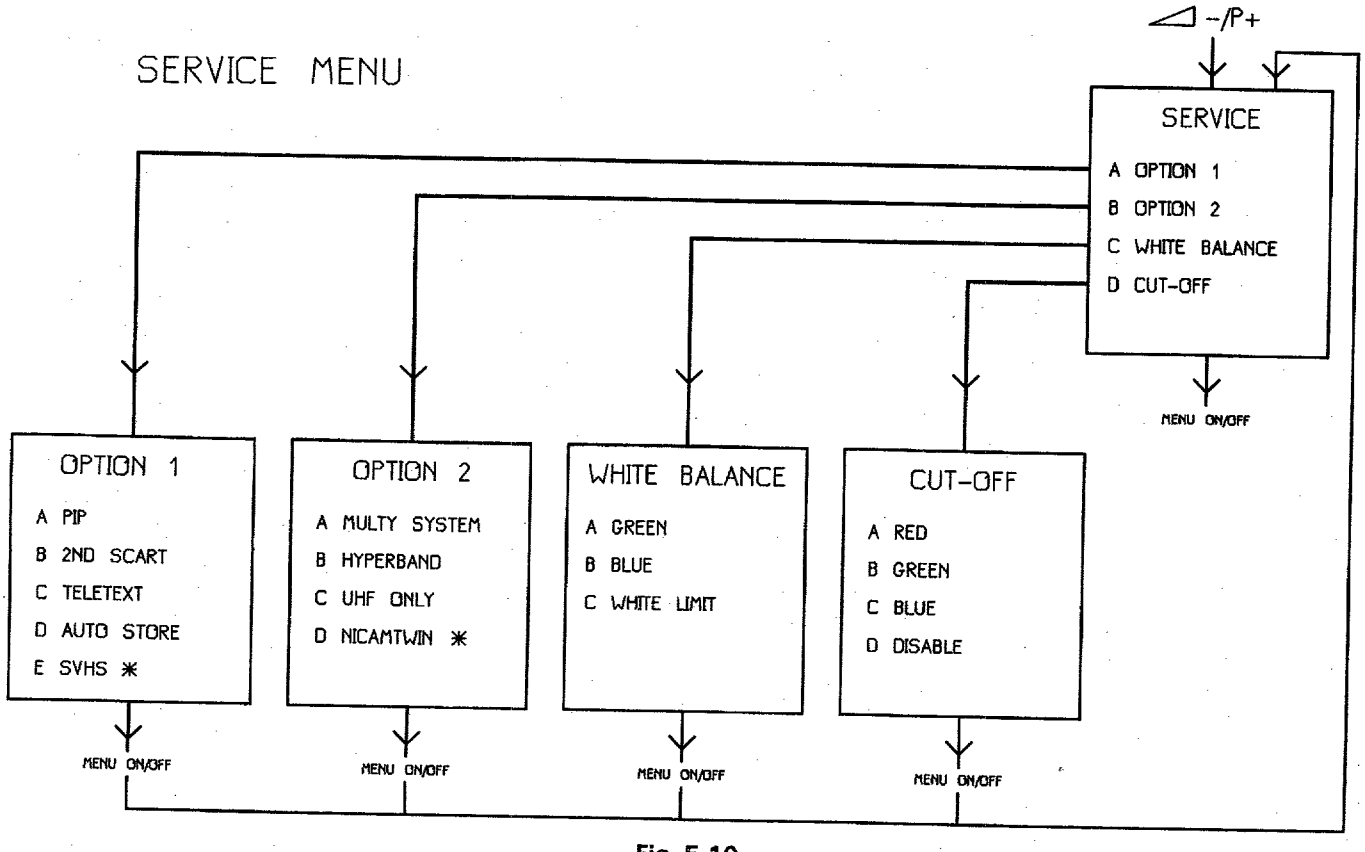


Fig. 5.10

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In IC7311 by means of the EXT2 signal a selection is made between CVBS from the IF/Sound module and the chrominance (C) and luminance (Y) signal from the SVHS connector EXT2.

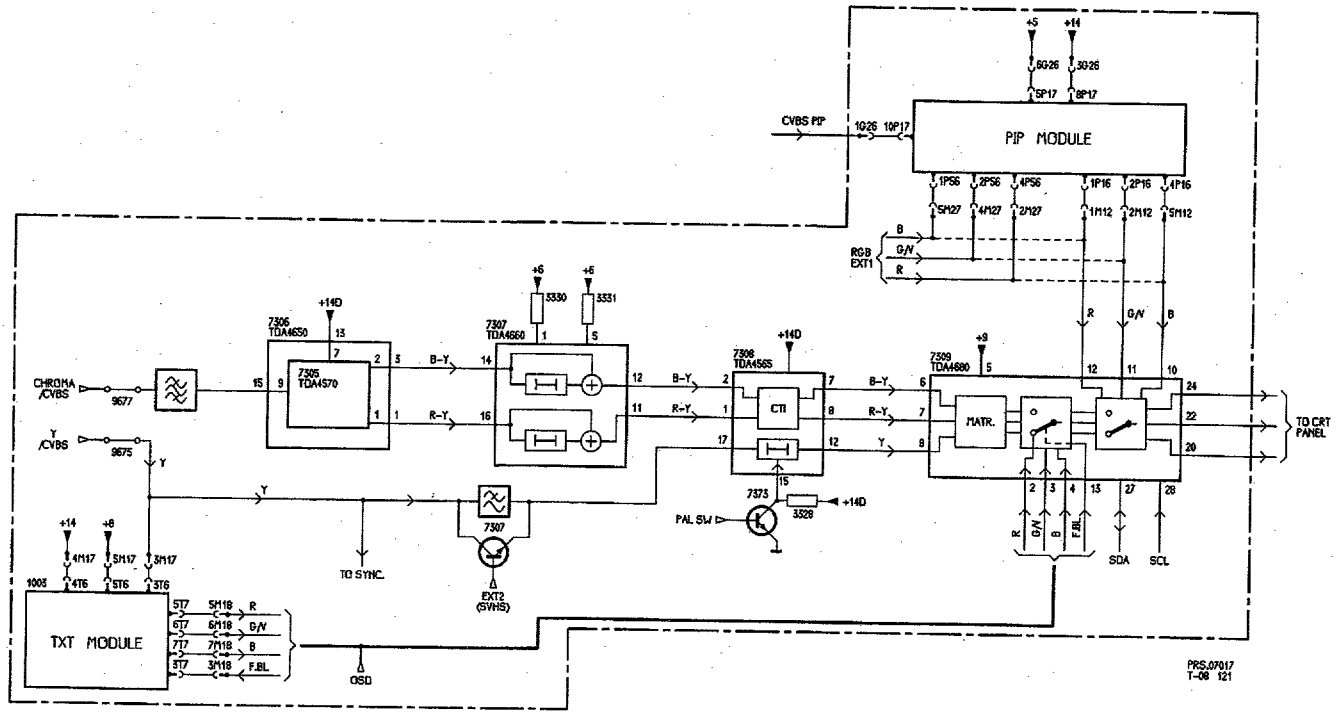


Fig. 5.1

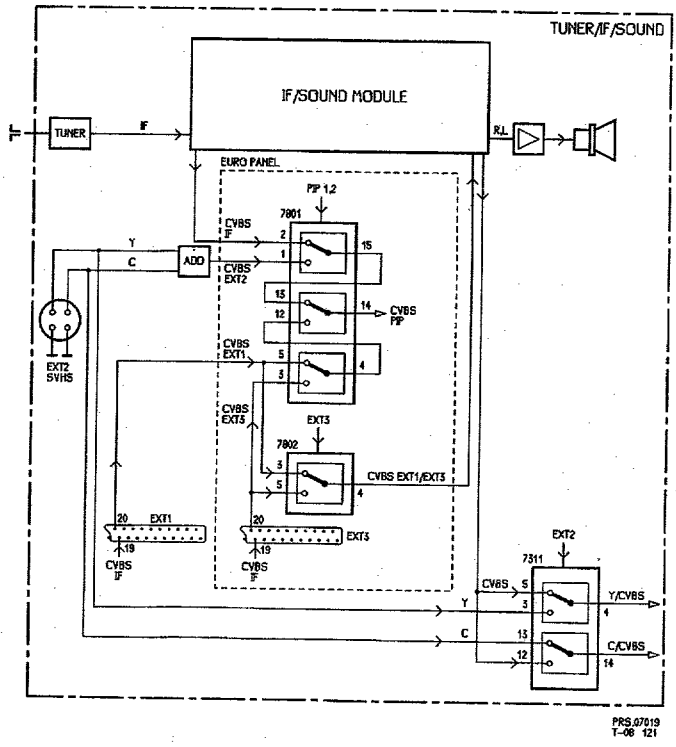


Fig. 5.2

# 5.3 The luminance path

The CVBS or Y-signal, from the video source selector switch IC7311, is supplied to a chroma bandstop filter which can be switched on (see fig. 5.3).
Two cases can be distinguished:

-PAL/SECAM
During PAL/SECAM operation the SVHS control signal (EXT2), coming from the microcomputer, is low. This blocks TS7303 and a filter composed of L5303/C2315/C2368 and C2320/R3307 filters the chroma signal from the CVBS signal.

-PAL/SECAM SVHS
In the case of a PAL/SECAM SVHS signal, the SVHS control signal (EXT2) is high, which causes TS7303 to conduct. The result of this is that the luminance signal (Y) is passed on via TS7303, which means that the filter is not active.

The luminance signal is then supplied to pin 17 of IC7308 (TDA4565) via a buffer TS7310.

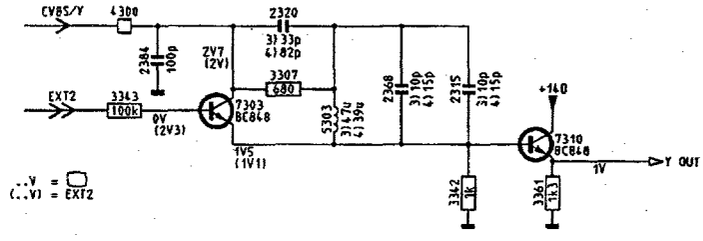


Fig. 5.3

## Luminantie vertraging in de TDA4565

The Y-signal, coming from the buffer TS7310, is supplied to pin 17 of the TDA4565 (TP5), the input of the luminance delay line. See fig. 5.4.
The delay of this delay line is set by means of a DC voltage at pin 15.
In the case of PAL (for MULTI-system units), the control signal (PAL SW) is high. This causes TS7373 to conduct, a low voltage is supplied to pin 15 and there is a shorter delay in the luminance channel.
In the case of single-system units, the TDA4565 is not used; the required luminance delay is now achieved using a separate delay line DL5306.

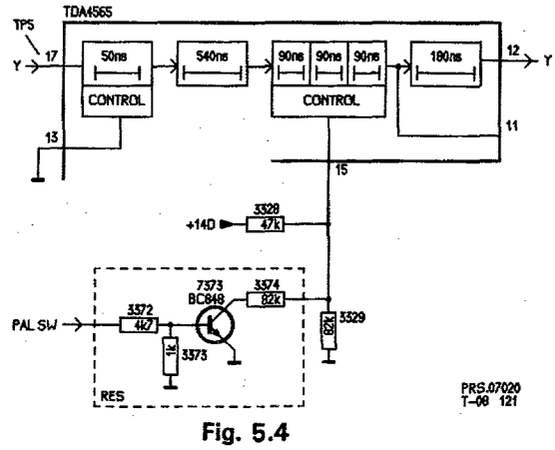


Fig. 5.4

# 5.3 The luminance path

The CVBS or Y-signal, from the video source selector switch IC7311, is supplied to a chroma bandstop filter which can be switched on (see fig. 5.3).
Two cases can be distinguished:

-PAL/SECAM
During PAL/SECAM operation the SVHS control signal (EXT2), coming from the microcomputer, is low. This blocks TS7303 and a filter composed of L5303/C2315/C2368 and C2320/R3307 filters the chroma signal from the CVBS signal.

-PAL/SECAM SVHS
In the case of a PAL/SECAM SVHS signal, the SVHS control signal (EXT2) is high, which causes TS7303 to conduct. The result of this is that the luminance signal (Y) is passed on via TS7303, which means that the filter is not active.

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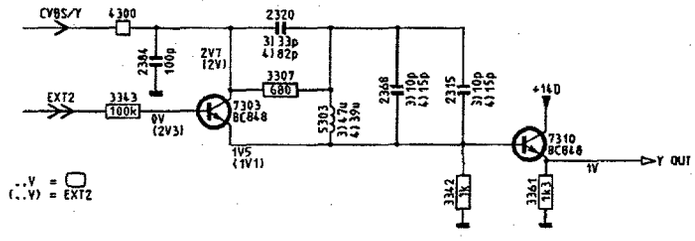


Fig. 5.3

## Luminantie vertraging in de TDA4565

The Y-signal, coming from the buffer TS7310, is supplied to pin 17 of the TDA4565 (TP5), the input of the luminance delay line. See fig. 5.4.
The delay of this delay line is set by means of a DC voltage at pin 15.
In the case of PAL (for MULTI-system units), the control signal (PAL SW) is high. This causes TS7373 to conduct, a low voltage is supplied to pin 15 and there is a shorter delay in the luminance channel.
In the case of single-system units, the TDA4565 is not used; the required luminance delay is now achieved using a separate delay line DL5306.

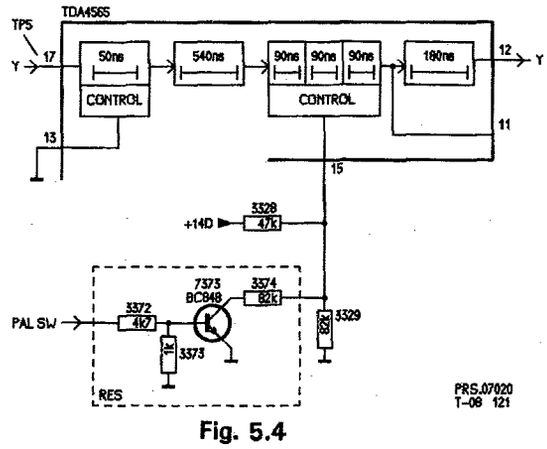


Fig. 5.4

In IC7311 by means of the EXT2 signal a selection is made between CVBS from the IF/Sound module and the chrominance (C) and luminance (Y) signal from the SVHS connector EXT2.

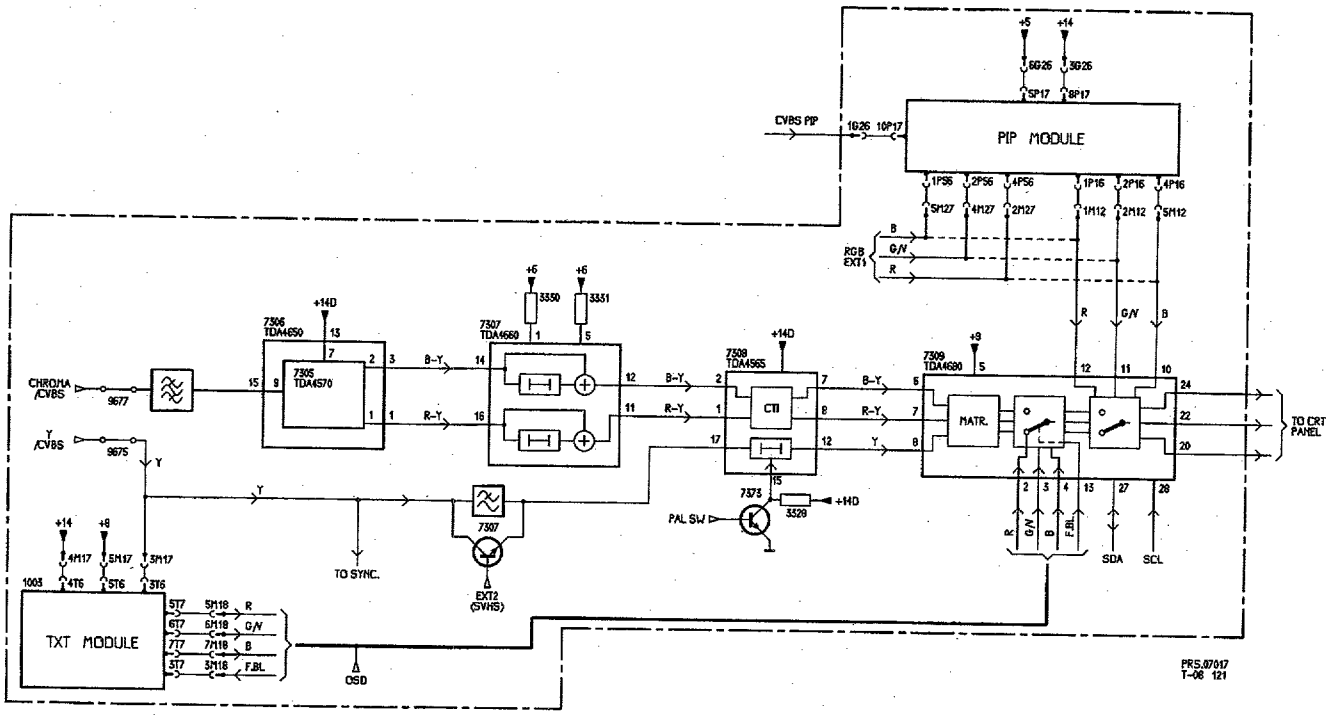


**Fig. 5.1**

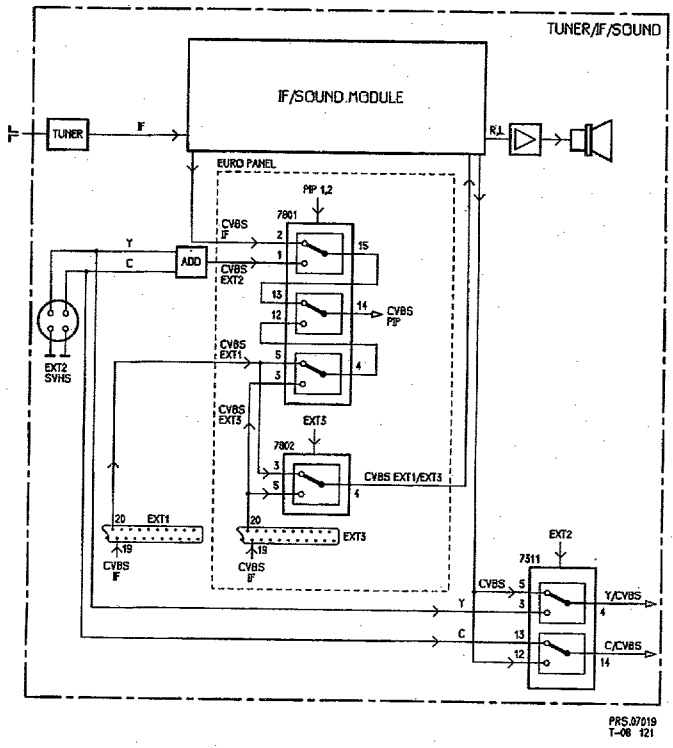


**Fig. 5.2**

# 5. The video path

Contents



## 5.1 The block diagram

The CVBS/CHROMA signal coming from the video source selector switch is supplied to IC7306 (or IC7305) via an input filter (see fig. 5.1). The demodulator in TDA4510 or TDA4650 demodulates the signals and has the R-Y and B-Y signals as outputs. These signals are sent to IC7307 (TDA4660), the base band delay lines. The R-Y and B-Y output signals of the delay lines are sent to IC7308 (TDA4565), the CTI-IC. The Y-signal, coming from the video source selector switch, is sent to the adjustable delay line in the CTI-IC via a bandstop filter which can be switched on. The delayed Y-signal and the colour difference signals are finally supplied to IC7309 (TDA4680), the video control, which converts the colour difference signals into RGB signals. There are also separate RGB inputs for RGB signals from EXT1 or PIP and for TXT or OSD signals. Moreover, the brightness, contrast and colour saturation control and also a cut-off point stabilisation take place in the video control IC.

## 5.2 Video source selection

The selection of the required video signal for both the main picture and the PIP picture takes place by means of IC7801 and IC7802 on the EURO panel and IC7311 on the chassis (see fig. 5.2).
Here the video signals may come from:

- The IF/Sound module (CVBS IF)

This CVBS signal is supplied to pin 2 of IC7801 and pins 19 of euroconnector 1 and euroconnector 3.

- Euroconnector 1 (CVBS EXT1)

This CVBS signal is supplied to pin 5 of IC7801 and pin 3 of IC7802. The CVBS status information at pin 8 (CVBS STATUS1) of this euroconnector is supplied to the microprocessor.

- SVHS connector 2 (CVBS EXT2)

The luminance and the chrominance signal are added together and supplied to pin 1 of IC7801. The luminance signal (Y) and the chrominance signal (C) are also supplied to pins 3 and 13 of IC7311.

- Euroconnector 3 (CVBS EXT3)

This CVBS signal is supplied to pin 5 of IC7802 and pin 3 of IC7801. The CVBS status information at pin 8 (CVBS STATUS3) of this euroconnector is supplied to the microprocessor.
By means of the PIP1 and PIP2 signals, a selection is made in IC7801 between CVBS IF/CVBS EXT2 and CVBS EXT1/CVBS EXT3. The selected output signal (CVBS PIP) is supplied to the PIP module. In IC7802 a selection is made between CVBS EXT3 and CVBS EXT1 by means of the EXT3 signal. The selected output signal CVBS EXT1/EXT3 is supplied to the IF/Sound module.

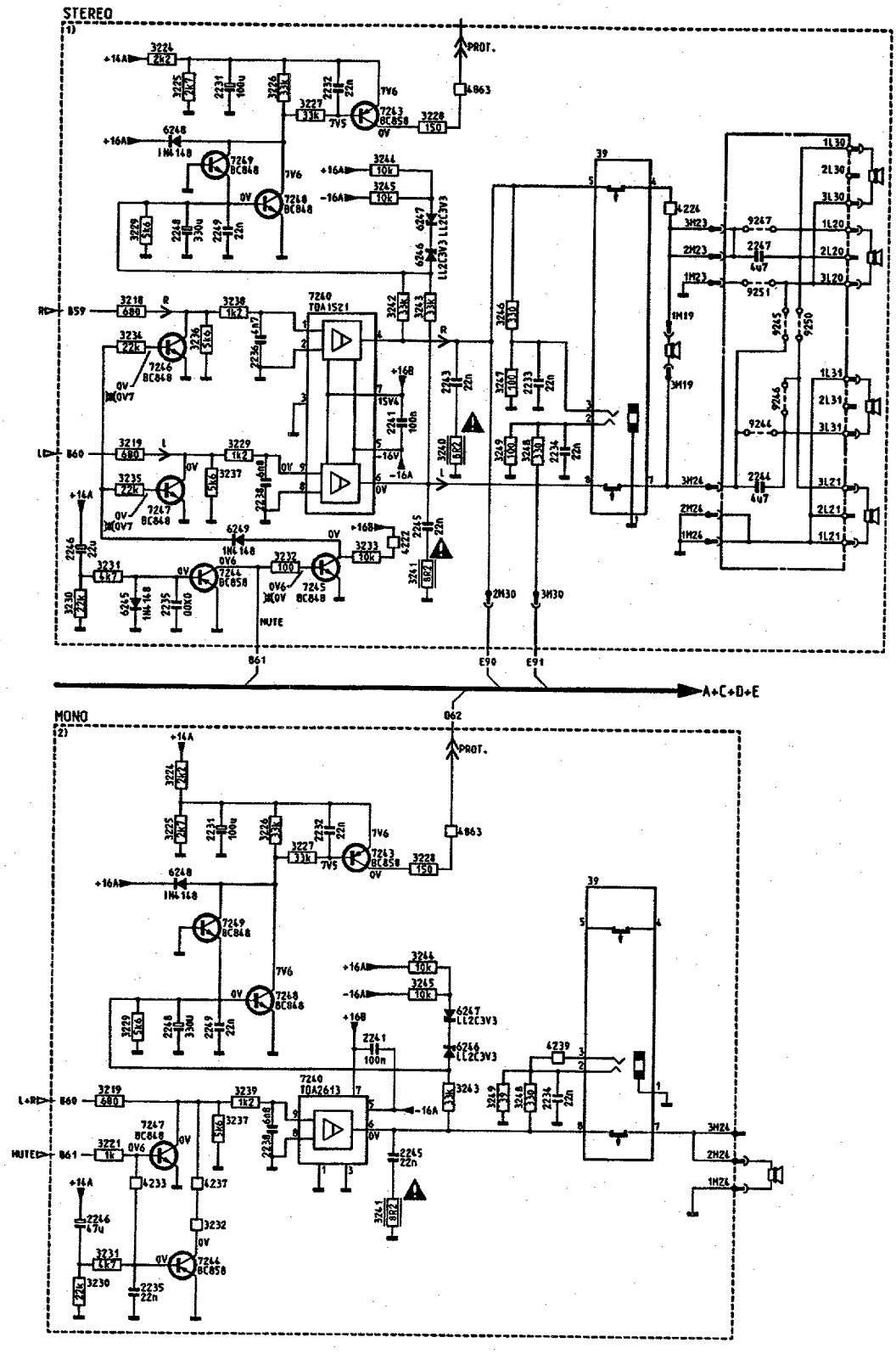


Fig. 4.9

## 4.4 Source selection external sound

External sound can be supplied to the unit in the following ways: (see fig. 4.8)

-- via euroconnector EXT1 (L EXT1 and R EXT1)
-- via euroconnector EXT3 (L EXT3 and R EXT3)
-- via connector EXT2 (L EXT2 and R EXT2)

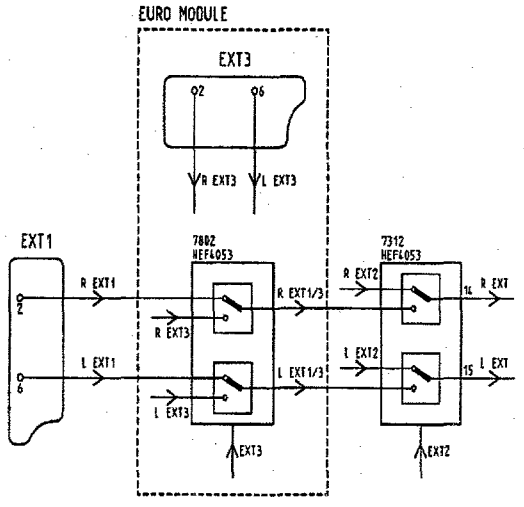


Fig. 4.8

Selection between the sound sources takes place as follows: On the EURO module a choice is made between the sound signal coming from euroconnector 1 or 3 via IC7802 (HEF4053) and using the EXT3 control signal. If euroconnector 3 is not present, the external 1 sound signals are sent directly to IC7312.
In IC7312 selection takes place between external sound from euroconnector 1/3 and external sound coming from connector EXT2 by means of the EXT2 control signal.
The output signals at pins 15 and 14 (L EXT and R EXT) are supplied to the intermediate frequency/sound module.
At each intermediate frequency/sound module a selection can be made between external sound or sound coming from TV reception.

## 4.5 The sound output apmplifiers

The sound signals (L and R) from the intermediate frequency/sound module are supplied to the sound output amplifier TDA1521 (or TDA2613) (see fig. 4.9). The amplified output signal is supplied to the loudspeakers and headphones.

### Protection

If one of the outputs of the sound output amplifiers is not 0V or the +16A or -16A is not correct, the protection (PROT) will be activated via TS7248 and TS7243 (see section "POWER SUPPLY").

### Anti-plop protection

An anti-plop circuit is present to prevent troublesome plops caused by switching on and off.

### Stereo units:

Capacitor 2246 is charged when the unit is switched on. TS7244 and TS7245 block, which means that the sound is interrupted via TS7246 and TS7247. The MUTE signal, coming from the STEREO module, cancels the interruption of the sound. When the unit is switched off, capacitor 2246 discharges. The result of this is that TS7244 starts to conduct and TS7245 blocks. The sound is now also interrupted via TS7247 and TS7246.

### In the case of mono units:

Capacitor 2246 is charged when the unit is switched on. This means that TS7247 conducts briefly and sound is interrupted. When the unit is switched off, C2246 discharges so that TS7244 starts to conduct and the sound is now also interrupted.

## The D/A converter (TDA1543)

IC7168 (see fig. 4.7) contains an $I^2S$ interface and two D/A converters. The $I^2S$ interface obtains the data from the left and right channels from the $I^2S$ signal and sends them to their respective DA converters. These convert the samples supplied into an equivalent current at output pins 6 (left) and 8 (right). Another reference flow is added internally to this current which comes to the outside via pin 7. This reference current lifts the zero-level of the output signals, which improves the dynamic range. With the signal of pin 7, this current can again be compensated in the analog filters.

## The analog filters

The output signals at pins 6 and 8 of the DAC (see fig. 4.7) are sent to two selective amplifier circuits.
A selective amplifier circuit consists of an operational amplifier (IC7170 or IC7180) and several passive components. The current at pin 2 (- input) is converted into an output voltage. The value of this current is however offset with regard to the actual value, because a current is added in the D/A converter. By supplying a direct current (from pin 7 of IC7168) to the + input (pin 3) of the operational amplifier, the offset is removed. The L.F. sound signal is now available at pins 7 of IC7170 (right) and IC7180 (left), and from here goes to the FM sound/NICAM sound selection circuit in IC7200.

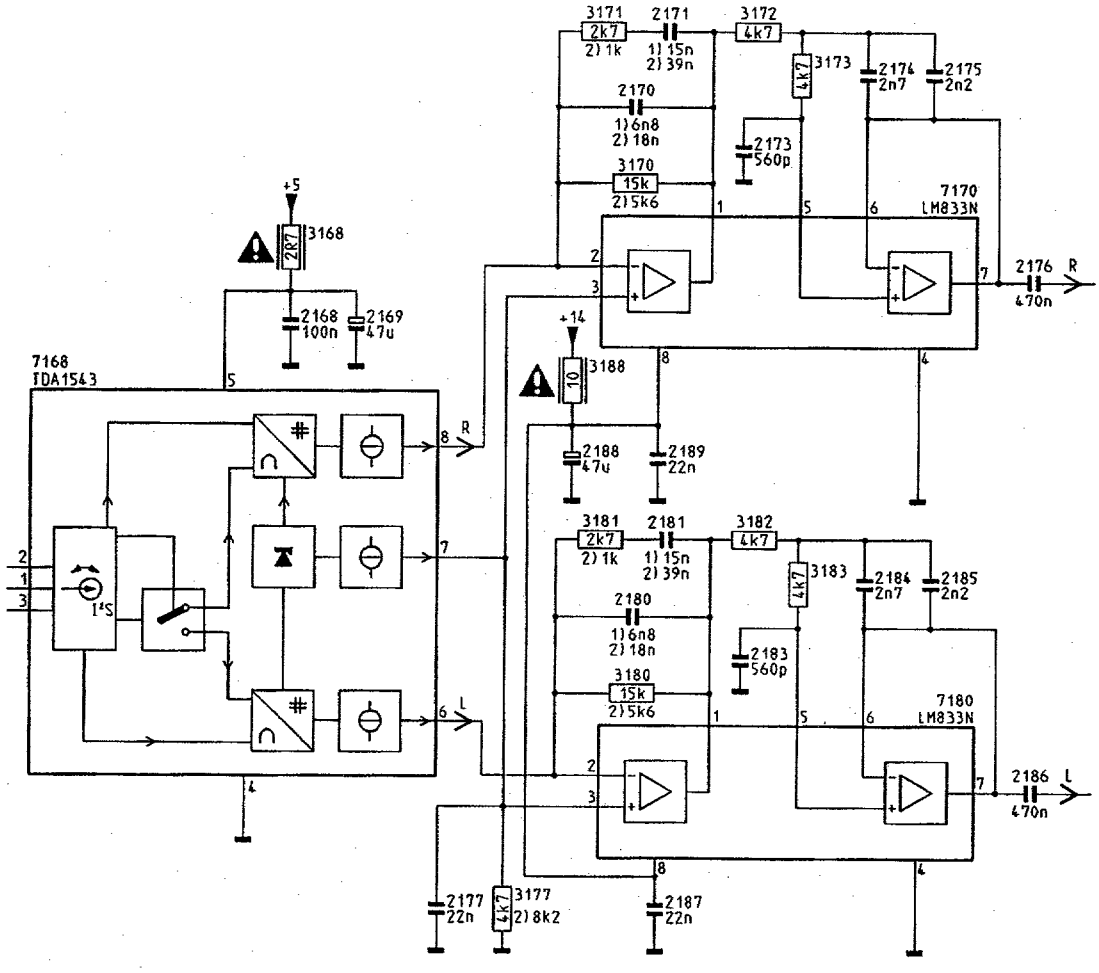


Fig. 4.7

# 4.3 Sound NICAM module.

Two sound paths can be distinguished on the NICAM intermediate frequency/sound module: an FM sound path for processing analog sound signals and a NICAM sound path for digital sound processing.

## The FM sound path

The FM sound path (see fig. 4.1) on the NICAM IF/sound module is almost identical to that on the Stereo IF/sound module. TDA8415 is now used instead of the stereo decoder (IC7200) TDA8417. The stereo decoder TDA8415 makes a selection between FM sound and NICAM sound, while the stereo decoder TDA8417 makes a selection between AM and FM sound.

## The NICAM sound path:

After intercarrier demodulation in the TDA3857, the NICAM intermediate-frequency signal is supplied to the NICAM input bandpass filter (1116) via pin 15 (see fig. 4.5).
The bandpass filter has a response frequency of 5.85 MHz for PAL BG or 6.552 MHz for PAL I. The NICAM phase-modulated sound signal remaining after filtering (PM sound) goes to pin 4 of the QPSK demodulator TA8662.

## The QPSK demodulator circuit (TA8662)

This circuit (see fig. 4.5) is responsible for the conversion of the phase-modulated carrier wave into a serial bitstream which again fulfils the NICAM format. The filtered phase-modulated signal is supplied to the AGC circuit. The output signal of the AGC circuit is supplied to the QPSK demodulator. The output signals of this demodulator are taken to the outside via pins 10 and 11. These signals are filtered by the lowpass filters L5129/C2129 and L5130/C2130. Via pins 20 and 19 the filtered data signals are supplied to the phase detector of the internal oscillator. The crystal type in the reference circuit depends on the system and is 6.552 MHz for PAL I and 5.85 MHz for PAL BG.
The filtered data signals continue to the differential encoder circuit. The NICAM coded signal at pin 29 is taken to the outside via a 2-bit parallel/serial converter.
Pin 18 is the output for the NICAM mute signal.
The 5.824 MHz clock signal is available at pin 26 and the 728 kHz clock signal at pin 27.

## The NICAM decoder (CF70123)

The NICAM decoder ensures that the serial digital information, coded according to the NICAM system, is converted once more into 14-bit words which can be processed directly by a D/A converter (see fig. 4.6).
The data signal is received at pin 23 and using the clock signal is read at pin 22. (The data signal of the QPSK demodulator is locked to the clock signal). The read signal is first descrambled. The descrambled data are taken to the outside via pin 7. The data signal on pin 7 is read directly at pin 15. The NICAM decoded signal is then converted into a signal according to the $I^2S$ format. This signal comes from the NICAM decoder IC via pins 3, 4 and 33 and goes to the DAC IC7168 (TDA1543). The NICAM control bits are present at pins 35 to 39. These control bits indicate what kind of signal is present (MONO/STEREO/TWO LANGUAGES). These control bits are sent to the microprocessor via the I/O expander (IC7160) and the $I^2C$ bus.

## Service tip

Using the colour pattern generator PM5515TN, PM5518TN or PM5518TNI, the QPSK demodulator and the NICAM decoder can be tested.
When test signal DATA1 is used, a pulse train can be measured at pin 29 of the QPSK demodulator. In this situation the NICAM decoder at pin 8 (ERFL) will also give a pulse train.
The test signal DATA2 is used to test the NICAM decoder. In this situation a 32 kHz pulse train can be measured on the $I^2S$ bus.

The test signal DATA3 gives an unmodulated NICAM sound carrier wave which is used for adjustments.

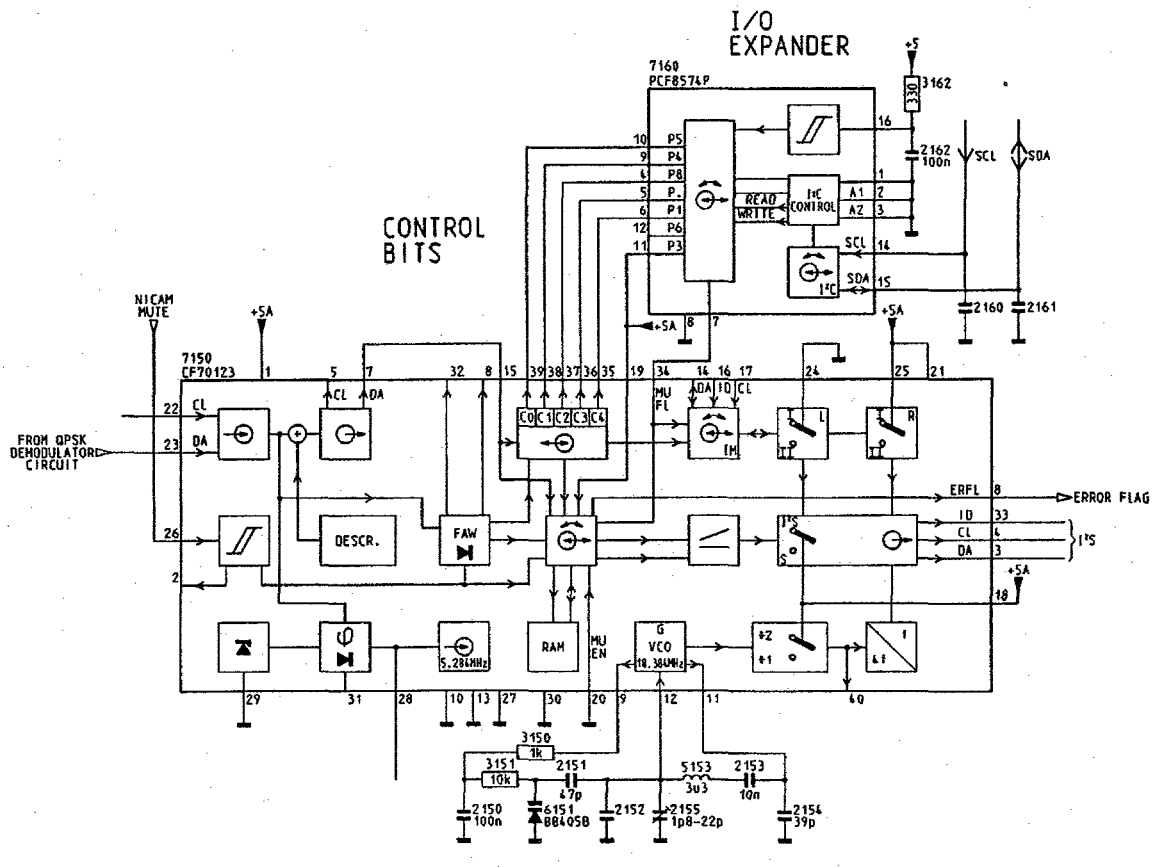


Fig. 4.6

# 9.3 Protected circuits

## Overvoltage protection

The supply circuit is protected against overvoltage via Zener diode 6663. If the voltage on capacitor 2660 (unstabilised +5) exceeds 17.5 V, the protected circuit will be energised and the supply circuit will be switched off.
If the +32 supply voltage exceeds 39.5 V, Zener diode 6666 will start conducting and the supply circuit will be switched off.

## High-voltage protection

If the line flyback pulse increases (and thus also the high voltage), for example as a result of a defect in the line circuit, Zener diode 6592 will start conducting and the supply circuit protection will be energised.

## Sound protection

The sound output amplifier is powered by means of a symmetrical power supply (+16 and -16). To prevent the loudspeakers from becoming defective if one of the supply voltages fails or if the outputs of the amplifier develop an internal short-circuit to one of the supply voltages, the +16 and -16 supply voltages and the outputs of the amplifiers are protected.
The DC level on the outputs of the amplifiers is measured via resistors 3242 and 3243 (in normal operation at 0V) and the DC level of the average of the +16 and -16 supply voltages is determined via resistors 3244 and 3245 (0V in normal operation 0V). A threshold of +/- 3.3 V is created via Zener diodes 6246 and 6247. In case of a positive or negative deviation from these DC levels, transistor 7248 or 7249 will start conducting, causing transistor 7243 to conduct as well. As a result the protection of the supply circuit is energised and the supply circuit is switched off.

## Beam-current protection

The beam current in principle runs through 3560 and is translated in a voltage across this resistor. If the voltage across this resistor increases (larger beam current), transistor 7591 will be driven into conduction via Zener diode 6590 and resistor 3590, thus energising the supply circuit protection.

## East-West protection

If, due to a defect of transistor 7533, the line circuit is no longer connected to the east/west modulator, the voltage on coil 5534 will increase. Zener diode 6561 will start conducting and the supply circuit protection will be energised.

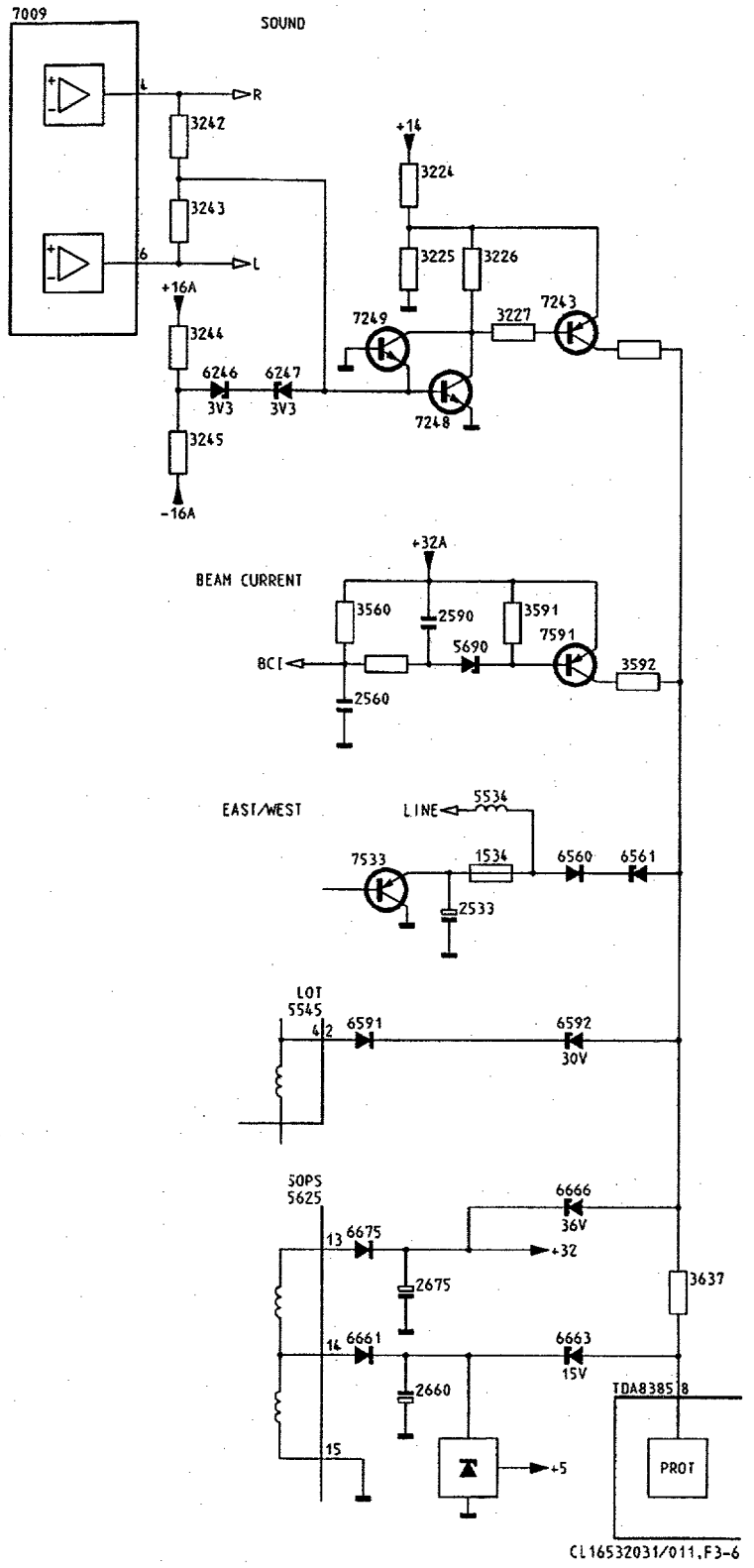
7009
SOUND
L
R
3242
3243
6
L
+16A
3244
6246
3V3
6247
3V3
3245
-16A
+16
3224
3225
3226
7249
3227
7243
7248
+32A
BEAM CURRENT
3560
2590
3591
7591
5690
BCI
3592
2560
EAST/WEST
LINE
5534
7533
1534
6560
6561
2533
LOT
5545
4
2
6591
6592
30V
SOPS
5625
6666
36V
13
6675
+32
2675
3637
14
6661
6663
15V
2660
15
+5
TDA8385
PROT
CL16532031/011.F3-6

Fig. 9.6

# 9.2 The secondary side

## The TDA8385

The TDA8385 is powered from winding 15-18. The supply voltage on pin 16 should be somewhere between 7.5 V and 20 V. As long as the supply voltage is below 7.5 V, the LED part of the opto-coupler will not be driven and the start-up of the supply circuit will be controlled by the opto-coupler.

## The sawtooth generator

The collector current of the switching transistor is measured indirectly, via winding 15-18 and R3647, on pin 12 of the TDA8385 and is stored in C2662. If the switching transistor is off, C2662 will be discharged via an internal switch, thus producing a sawtooth voltage across C2662. The size of the sawtooth voltage thus is a representation of the size of the collector current through the switching transistor.

## The pulse width modulator

The output voltage of the supply circuit (+148 supply) is fed back to pin 9 via resistors 3631, 3634 and 3635, and compared with the sawtooth voltage from the sawtooth generator. As soon as the sawtooth voltage exceeds the voltage measured, the output of the pulse width modulator will go HIGH and the LED will be switched on. The switching transistor will be turned off.

## Slow-start mechanism

A slow-start mechanism improves the reliability of the supply circuit during start-up. Capacitor 2664 is charged slowly during the start-up of the supply circuit. The voltage level of this capacitor is a reference for the maximum collector current that may run through the switching transistor. The maximum voltage level of this capacitor is clamped at the feedback voltage on pin 9. As a result the slow-start mechanism also functions after an overload, short-circuit or stand-by of the supply circuit.

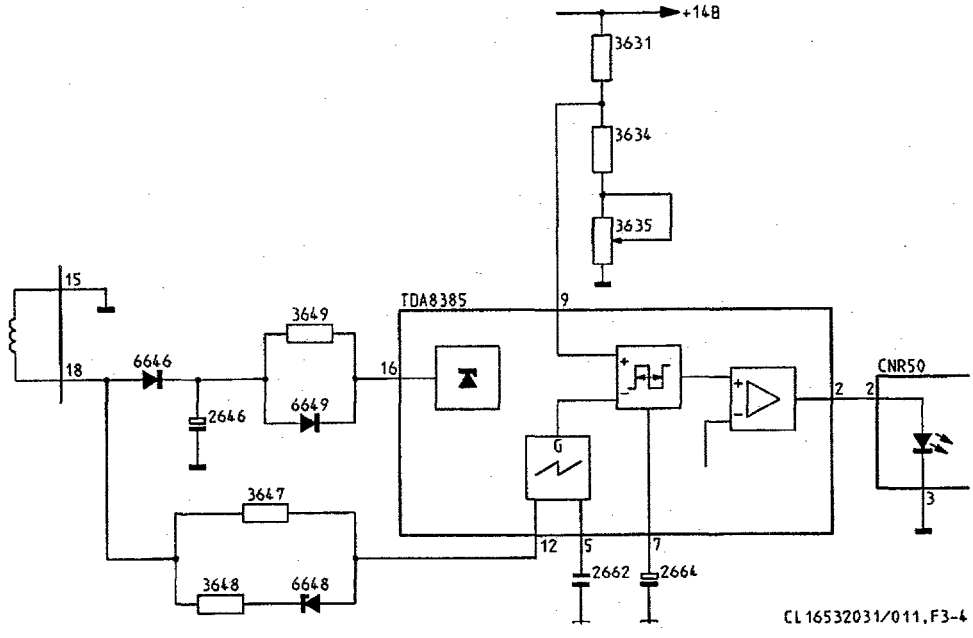


Fig. 9.4

## Stand-by

During stand-by, thyristor 6670 (see Fig. 9.5) is driven into conduction and the +5 supply is powered from winding 13-15 (+32 supply). The voltage on winding 13-15 is approximately 3 times the voltage across winding 14-15 during normal operation. This voltage is measured on pin 10. If this voltage exceeds 2.5 V, the LED will be switched on and the switching transistor turned off. In addition, transistor 7672 will be driven into conduction, causing slow-start capacitor 2664 to be discharged. The LED remains ON until the voltage on pin 10 drops below 2 V. The supply circuit then is released and begins to start up again until the voltage on pin 10 exceeds 2.5 V again.
Consequently, all the supply voltages of the SOPS, except the +5, will be a factor of three lower.
To ensure a good functioning of the IC in stand-by, the power supply of the IC will be taken over on pin 16 via diode 6660.

## Protection

Error situations are reported on pin 8 of the TDA8385 (see Fig. 9.6). If the voltage on pin 8 exceeds 2.5 V, the slow-start capacitor will be discharged. This causes the switching transistor to be turned off until the voltage on pin 8 drops below 2.5 V. The supply circuit will be started up again. If a protection is still active, the procedure will be repeated.

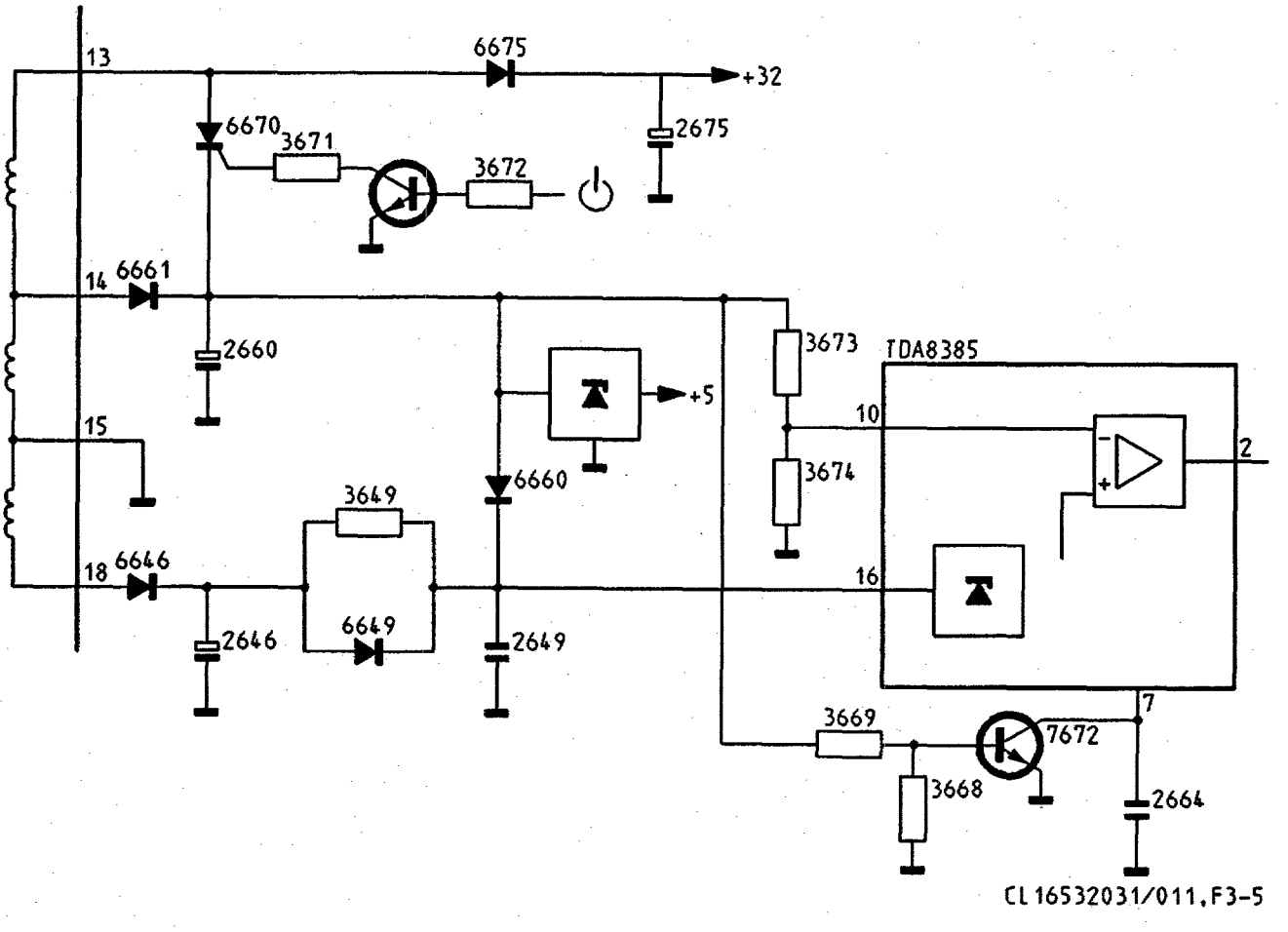


Fig. 9.5